PRELIMINARY DATA SHEET

Description: The 43Gb/s clocked-driver module includes in a same compact package, a driver, a 3R function (Re-shaping, Re-amplifying, Re-clocking), a clock-frequency doubler and a clock/data phase alignment. The package is with GPPO miniature connectors.

Main features :

- 14-Pin package with input/output GPPO connectors
- Differential output
- Ultra-high speed data rate: 43 Gbit/s
- Output adjustable voltages / channel: (2.8 – 3.6 Vpp)
- 12 ps of Clock-Phase-Margin @ 43 Gb/s
- Low output voltage rms jitter (600 fs) independent of data-input jitter
- Consumption max: 5.5 W @ 3.6 Vpp / channel
- 21.5 GHz input clock signal

Applications :

- 43Gb/s optical modulator driver for DPSK transponder in long haul DWDM transmission

Enclosed data :

1. Absolute Maximum Rating
2. Electrical characteristics
3. Digital measurement @ 43 Gb/s
   - Eye diagrams
   - BER (OSNR) in back-to-back
4. Outline drawings & Pin allocation

1. Absolute Maximum Ratings

N°	PARAMETER	CONDITIONS	SYMB	MIN	MAX	UNIT
1	Operating Case Temperature		Tc	0	+75	°C
2	Operating Relative Humidity	Non condensing	RHop	5	90	%
3	Operating Ambient Temperature	a) With no air flow b) Forced convection 1 m/s linear	Ta_n Ta_af	-5 -5	+30 +55	°C
4	Storage and Transportation Temperature	Non condensing	Tstg	-40	+75	°C
5	Storage Temperature 72 h max	Non condensing	Ttrs	-40	+85	°C
6	Storage and Transportation Relative Humidity	Non condensing	RHst	5	95	%

2. ELECTRICAL characteristics

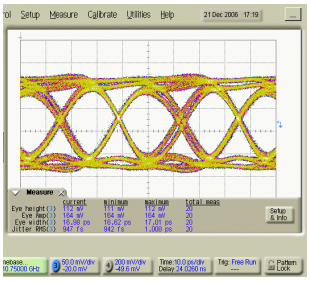
N°	PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
1	Input Data rate		F_B	42.0	43.018	45.3	Gbit/s
2	Input clock frequency		F_{clk}	21.0	21.509	22.65	GHz
3	Output data rate		F_B	42.0	43.018	45.3	Gbit/s
4	Data input return Loss	100KHz- 50MHz 50MHz - 38GHz 38GHz - 50GHz	S_{11}			-15 -10 -8	dB
5	Clock input return loss	21/22.65GHz	S_{11}			-10	dB
6	Output Return Loss	100KHz- 50MHz 50MHz - 50GHz	S_{22}			-15 -10	dB
7	Data Input amplitude range	Single-ended	VSD_{in}	325		550	mV
8	Clock Input amplitude range	Single-ended	VCK_{in}	325		750	mV
9	Clock input duty cycle tolerance			45		55	%
10	Input phase margin		In_{PM}	6	12	14	ps
11	Output amplitude range	Single ended, not inverted	VD_{out}	2.8	3.2	3.6	V
12	Data output vertical eye opening		vEO_{out}	75			%
13	Data output horizontal eye opening		hEO_{out}	80			%
14	Output Rise & fall Time, single ended		T_{SR}/T_{SF}		10	11	ps

15	Output Rise & fall Time differential		T_{DR}/T_{DF}		8	9	ps
16	Output jitter (peak-to-peak)		J_{pp}		3.4	4.5	ps
17	Output jitter (rms)		J_{rms}		600	800	fs

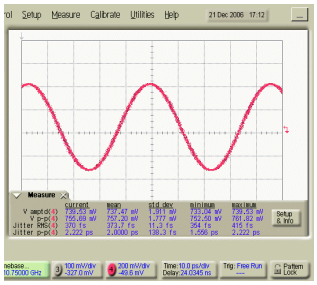
3. Digital measurements

3.1 Eye diagram @ 43 Gb/s T_{Case} = 25°C

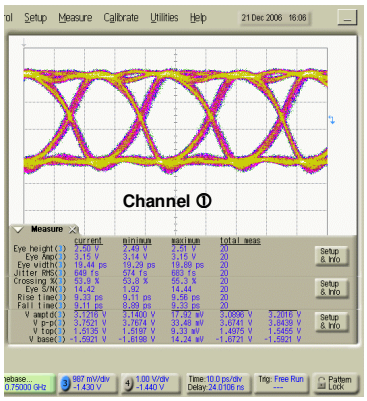
Input data@43G#150mV

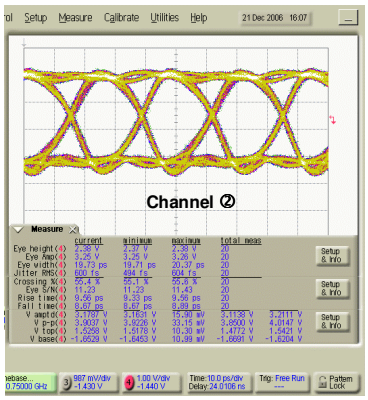


Input clock@21.5G#750mV



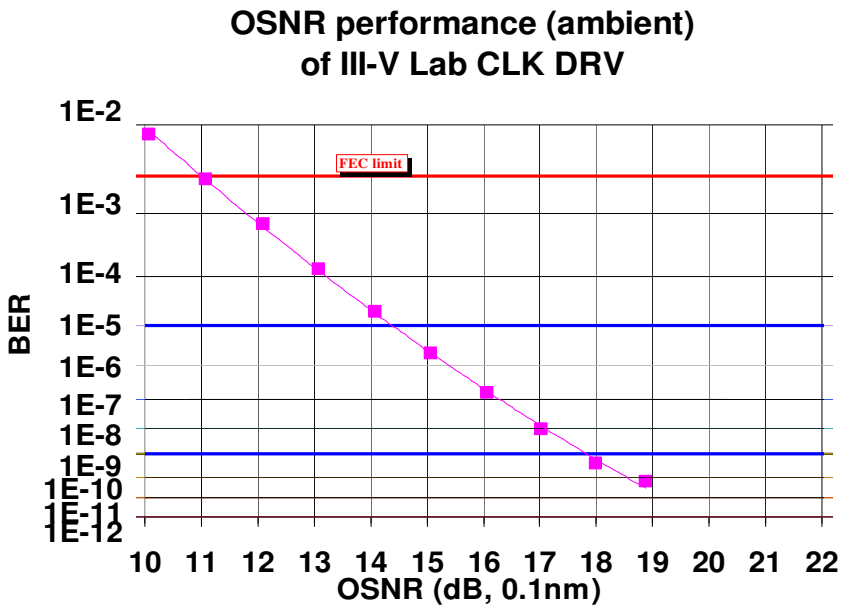
Typical output amplitude#3.2V



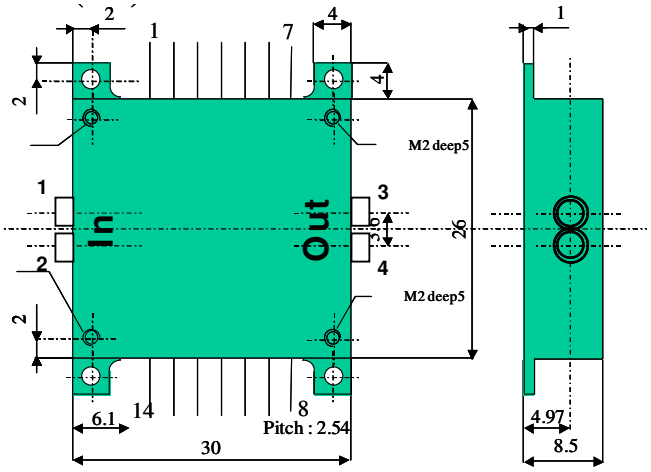


Note: **The output signal quality, compared to that of input signal, shows the strong interest of a clocked-driver**

3.2 Back-to-back Bit-Error-Rate versus OSNR (Optical Signal to Noise Ratio): state-of-the-art



4. Outline drawings & Pin allocation



Pin	Description	Voltage (V)	$I_{Max.}$ (mA)	$I_{Typ.}$ (mA)
1	Power Supply	-4.2	350	300
2	Power Supply	-2.3	250	230
3	Power Supply	+2.9	50	40
4	Power Supply	-5.2	220	200
5	Power Supply	-5	100	80
6				
7				
8	Power Supply	-3.2	350	310
9	Power Supply			
10	Power Supply	+7	250	200
11	Power Supply			
12	Power Supply			
13	Phase control	-2.5 ➔-3.5	5	2
14	Phase control	-3.5 ➔-2.5	5	2

GPPO	Description
1	Data in
2	Clock in
3	Data out
4	Inverse Data out