CDR with loop filter

86G CDR 1:2 Demux

MICRAM MICROELECTRONIC

Type: Module	Technology: SiGe	f_T/f_{max}: 225/300 GHz	Metallization: 4	Ref.-No.:R1020

Brief description:

The CDR consists of an input amplifier, a PD with data recovery, a 1:2 demultiplexing functionality and a delay line. Two output clocks providing the driving clock frequency and clock/2 are available for easier data processing off chip. The external loop filter (LF) is dimensioned for operation with a 54GHz TLC VCO and its expected tuning sensitivity. The loop filter settings have to be customized after measurement of the exact VCO characteristic by the customer. Standard setup is the CDR module with the loop filter board on top of it. A separate VCO module (not in shipment) has to be connected by the customer. Note that the VCO output must be connected to the CDR clock input via an attenuator in order to protect the CDR clock input.

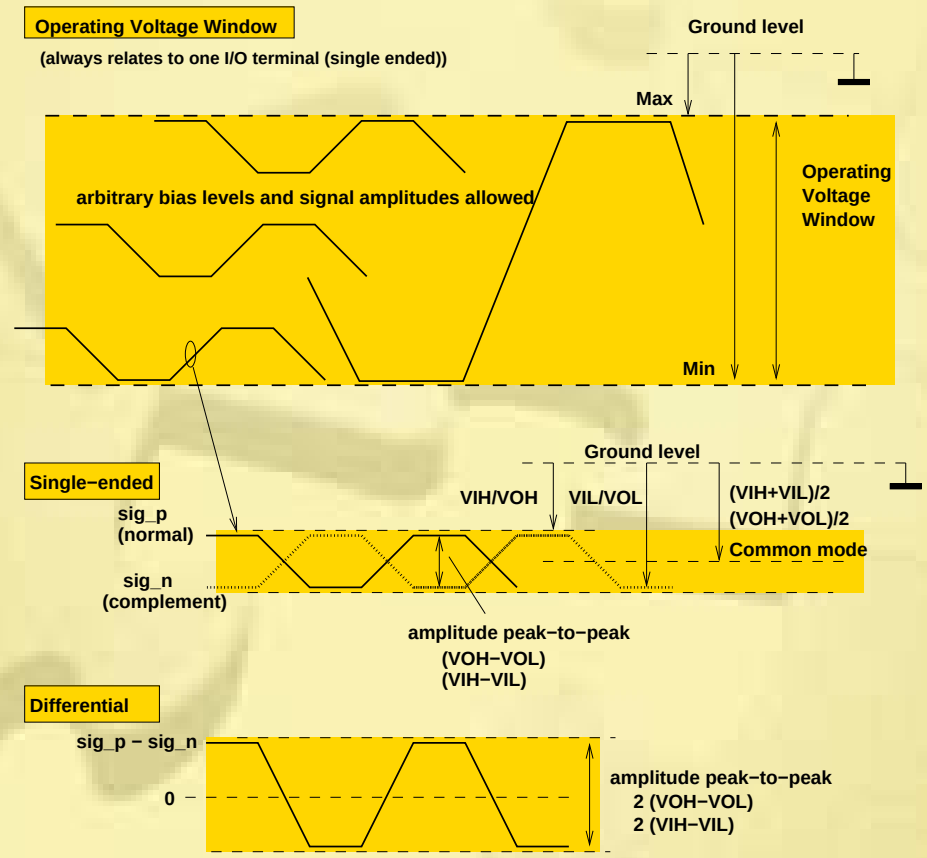
Electrical data:

Parameter	Symbol	Min	Typ	Max	Unit	Remark/Condition
General operating conditions						
Junction temperature range		0		+125	°C	
Ambient temperature range		0		+50	°C	
Current consumption of CDR			1100		mA	
Current consumption of LF			4×20		mA	
Power supplies						
Power supply of CDR	V_{ee}		-5.0		V	
Power supplies of LF	$V1p$		+5.0		V	
	$V1n$		-5.0		V	
	$V2p$		+9.5		V	initial values, tunable
	$V2n$		-0.5		V	initial values, tunable
Absolute maximum ratings of LF power supplies	$V1p$	0.0		+10.0	V	
	$V1n$	-10.0		0.0	V	
	$V2p$	0.0		+16.0	V	
	$V2n$	-16.0		0.0	V	
LF voltage window 1	$V1p$-$V1n$		+10.0	+10.0	V	required for operation
LF voltage window 2	$V2p$-$V2n$		+10.0	+10.0	V	required for operation
PLL operation with TLC VCO						
Input data rate of CDR			86		Gbit/s	
Expected PLL locking range			±200		MHz	
Expected PLL bandwidth	BW		5		MHz	
Push-button from upP to GND			open			when PLL is locked temporary for obtaining PLL lock
			GND			
LF output voltage (V_{tune})	VO	+4.6		+6.4	V	single ended, valid for initial values of $V2p$ and $V2n$
Expected VCO tuning voltage (V_{tune})	VI	0		+18	V	single ended, expected for TLC VCO

Parameter	Symbol	Min	Typ	Max	Unit	Remark/Condition
RF data inputs of CDR (DataInP, DataInN)						
Input amplitude	VIH-VIL	150	300		mV	single ended, peak-to-peak
Operating voltage window	VI	-700		300	mV	single ended
Input resistance	R		65		Ω	
RF clock inputs of CDR (ClkInP, ClkInN)						
Input amplitude	VIH-VIL	150	300		mV	single ended, peak-to-peak
Operating voltage window	VI	-700		300	mV	single ended
Input resistance	R		65		Ω	
RF data outputs of CDR (DataOut0P, DataOut0N) (DataOut1P, DataOut1N),						
Output amplitude	VOH-VOL		280		mV	single ended, peak-to-peak
Output resistance	R		65		Ω	
RF clock outputs of CDR (ClkP, ClkN)						
Output amplitude	VOH-VOL		280		mV	single ended, peak-to-peak
Output frequency	f		26.75		GHz	Equals input frequency
Output resistance	R		65		Ω	
RF half clock outputs of CDR (ClkHalfP, ClkHalfN)						
Output amplitude	VOH-VOL		280		mV	single ended, peak-to-peak
Output frequency	f		13.375		GHz	Half input frequency
Output resistance	R		65		Ω	

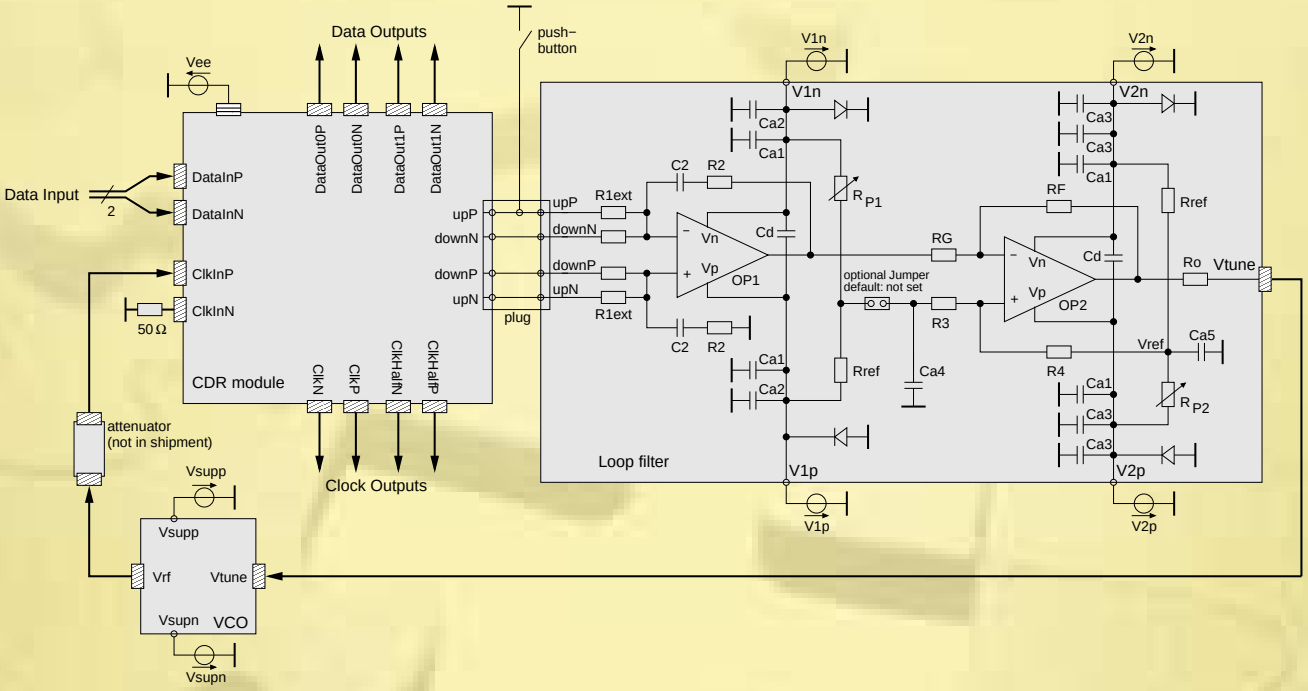
Signal definitions:

Definition of Voltage Levels and Amplitudes



PLL block diagram:

PLL with CDR, LF board and external VCO



Connecting the modules:

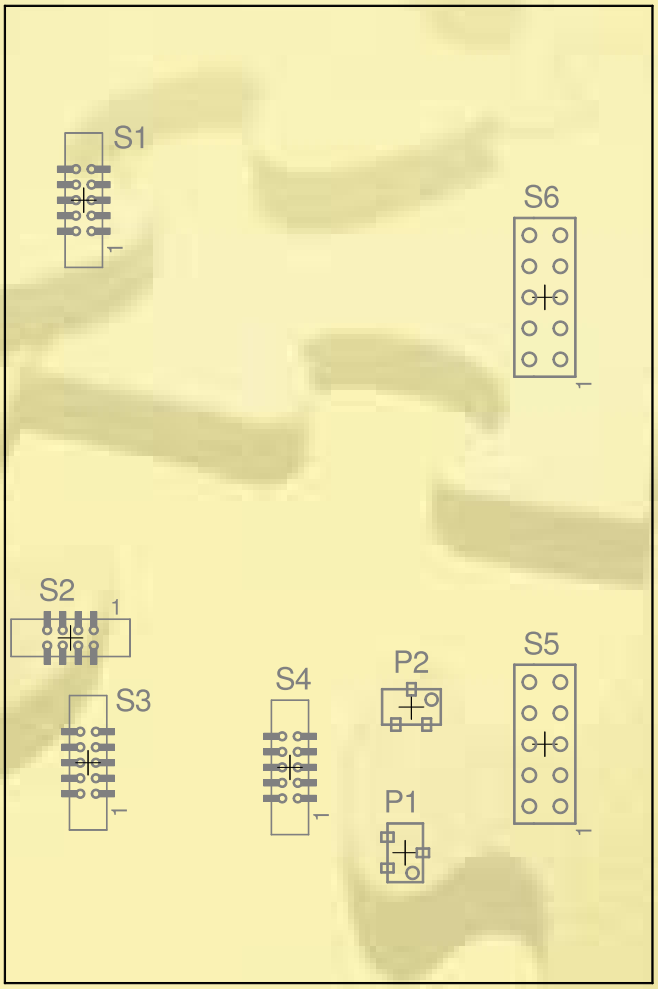
Connect the CDR / Loop filter module and the VCO as shown in the PLL block diagram. Please make sure to insert an attenuator if necessary to protect the clock input of the CDR. Exceeding the maximal allowed clock input value will damage the CDR permanently. The factor of attenuation depends on the output signal amplitude given by the VCO. Please determine first the VCO output amplitude and the necessary attenuation before connecting the VCO to the CDR.

Plug connectors:

Following pins provided by the plug connectors shown in the picture below must be connected:

Plug	Pin on plug	Connection
S1	3	V_{ee}
S2	4	Push-button to GND
S6	1	$V2p$
S6	2	$V2p$
S6	3	$V2n$
S6	4	$V2n$
S6	5	$V1p$
S6	6	$V1p$
S6	7	$V1n$
S6	8	$V1n$
S6	9	GND
S6	10	GND

All other pins should be not connected, so the plug connectors S3, S4 and S5 are not connected at all. These pins maintain connections to the CDR chip resp. loop filter, but are not necessary for PLL operation.



Plugs and potentiometers on the loop filter board.

Cooling:

It is recommended to apply cooling plates for the system, especially for the VCO.

Power up sequence:

1. Connect CDR, loop filter and VCO to GND.
2. Set all power supplies to 0V and connect VCO, CDR and loop filter to power supply.
3. Apply the specified VCO supply voltages. (Read in the VCO specification the voltage values and the exact rules for the VCO power up sequence.)
4. Apply $V1n$, $V1p$, $V2n$ and $V2p$ to the loop filter board. Take care not to exceed the 10V voltage window for $V1p$-$V1n$ resp. $V2p$-$V2n$.
5. Apply V_{ee} to the CDR block.
6. Wait until temperature of the system settles, so that circuit parameters are constant.

Power down sequence:

Disconnect the power supplies in opposite direction to the power up sequence, that is:

1. Decrease CDR supply V_{ee} to 0V.
2. Decrease loop filter supplies $V1n$, $V1p$, $V2n$ and $V2p$ to 0V. Take care not to exceed the 10V voltage window for $V1p$-$V1n$ resp. $V2p$-$V2n$.
3. Decrease VCO supplies to 0V. (Read in the VCO specification the exact rules for the VCO power down sequence.)
4. Disconnect all supply leads.

Operation:

First of all the customer has to perform a measurement of the VCO alone and determine the specific tuning voltage V_{tune} that gives the desired VCO output frequency. Then the output voltage range of the loop filter has to be adjusted so that the desired V_{tune} is settled roughly in the middle of it.
After applying the input signal to the data input of the CDR, press the push-button to acquire PLL lock. If the PLL doesn't lock, the PLL is in a condition where the loop filter cannot deliver the VCO tuning voltage V_{tune} which is necessary for the required frequency. This can occur in the initial condition of the loop filter, because the specified loop filter supply voltages $V2p$ and $V2n$ are initial values that have to be adjusted to customer's VCO. So the customer should perform first an adjustment of the loop filter before closing the phase locked loop.
In the following is described how the loop filter output voltage range can be adjusted.
The PLL block diagram above shows that the loop filter consists of two opamp stages. The second stage is an amplifier of factor 0.22, which additionally produces a shift of output voltage range. The output voltage range is shifted by means of adjusting the reference voltage V_{ref} of the second opamp stage, that is the potential on positive opamp input. Assuming an ideal output operating point of the first loop filter stage, i.e. 0V, the output operating point of the second stage is described by $V_{tune} = 1.22 \times V_{ref}$. V_{tune} in this equation is the middle value of the available VCO tuning voltage range, that covers about $\pm 600mV$ around this middle value. The equation shows that shifting V_{ref} will shift the available VCO input voltage range accordingly.
The reference voltage V_{ref} can be adjusted in two manners:

1. The supplies $V2p$ and $V2n$ of the second loop filter stage can be shifted, always maintaining the voltage window $V2p$-$V2n = 10$V. If the potentiometer P2 stays in default setting, i.e. $R_{P2} = R_{ref}$, V_{ref} is just the midpoint of the supplies:
   $V_{ref} = (V2p - V2n)/2$.
   Take care not to overstep the specified absolute maximum ratings of $V2p$ and $V2n$. If it should be necessary to set $V2n > 0$, please remove the protection diode which is placed on the loop filter board between $V2n$ and ground.
2. The potentiometer P2 can be tuned, which gives the reference voltage:
   $V_{ref} = V2n + (V2p - V2n) \times R_{ref}/(R_{ref} + R_{P2})$.
   R_{ref} has the value 560Ω, and R_{P2} can be tuned between 0 and 1kΩ. The default setting is $R_{P2} = R_{ref}$.

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