ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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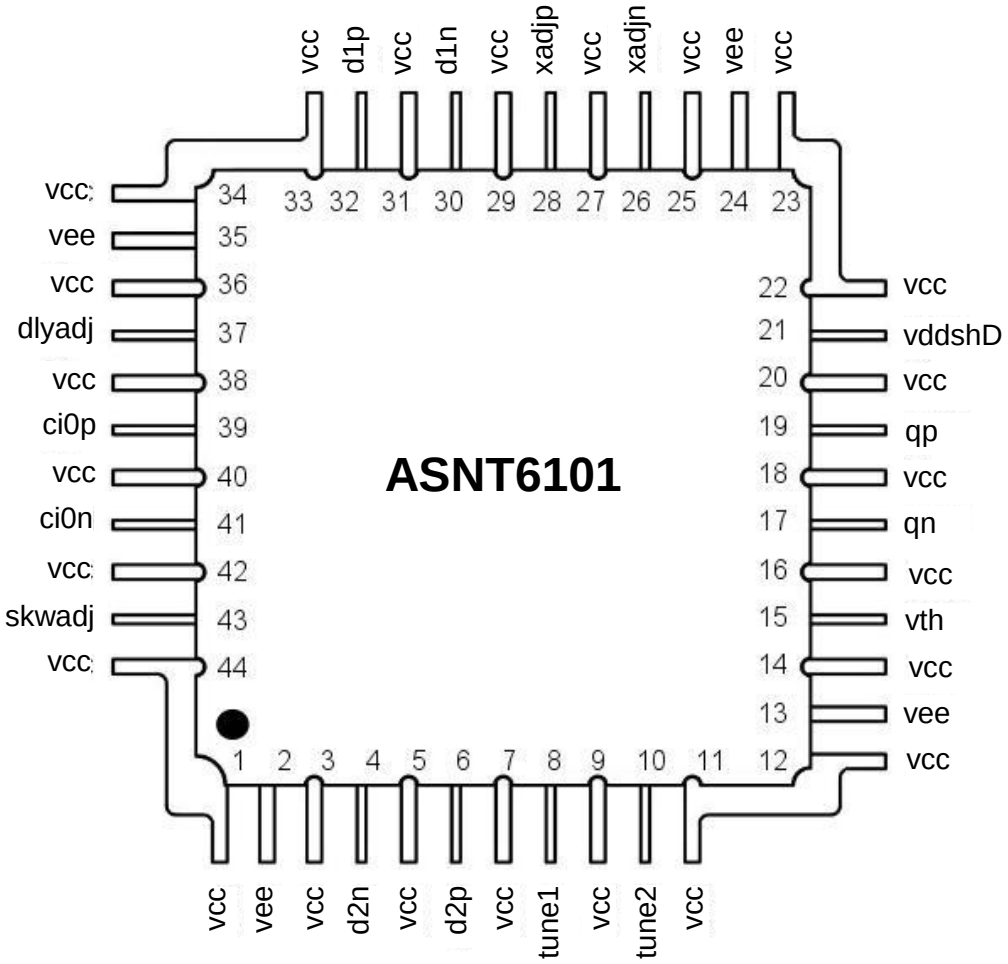
ASNT6101-KMM
53*Gb/s* - 26.5*Gbaud/s* PAM4 Signal Generator / Encoder

- High-speed two input binary data signals to one PAM4 output signal
- Adjustable data output amplitude for all 3 levels and eye quality control
- Single-ended output data eye cross point adjustment
- Opposite and parallel timing adjustment of the main clock vs. both data inputs
- Fully differential CML input and output data, and clock interfaces
- Single power supply of 3.6*V*
- Average power consumption: 1.25*W*
- Custom CQFP 44-pin package



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DESCRIPTION

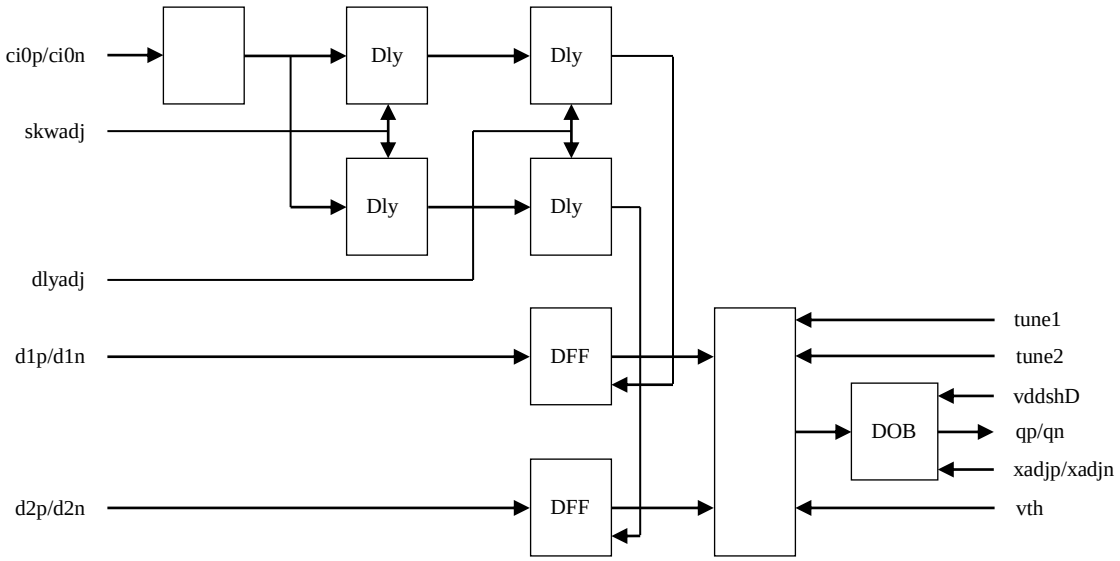

Fig. 1. Functional Block Diagram

The ASNT6101-KMM SiGe IC shown in Fig. 1 is a single lane PAM4 encoder. It takes two binary input data signals d1p/d1n, and d2p/d2n, retimes them with the input clock ci0p/ci0n, and then combines them into a 4 level output signal (PAM4) qp/qn. The input data rates in *Gbps* should be equal to the input clock frequency in *GHz*. The output data symbol rate will be equal to the input data symbol rate, but deliver twice the amount of data due to the multiple levels (i.e. twice the input data bit rate). For example, if the input data and clock are at 20*Gb/s*, and 20*GHz* respectively, then the output signal will be running at 40*Gb/s*-20*Gbaud/s*.

The input clock ci0p/ci0n is initially split into two identical paths comprising of several delay adjustable stages. Using skwadj, the delays of the two clock paths can be changed with respect to each other where one path's delay is increased while the other path's delay is decreased (or opposite). Both of the clock lanes can be delayed by more or less equal amounts using the control pin dlyadj. These two adjustment pins allow for proper alignment of the clock to the two input data signals at the two re-timing internal D-type flip flops DFF.

After the DFFs, the two signals are combined into a PAM4 signal where d1p/d1n is the MSB, and d2p/d2n is the LSB. External pins tune1, and tune2 can be used to separately adjust the amplitudes of the 3 upper signal levels in the PAM4 signal (i.e. independently adjust the weights of the MLB and the LSB). Pin tune1 adjusts the weight of d1p/d1n's contribution to the PAM4 signal while pin tune2 adjusts the weight of d2p/d2n's contribution. Pin vth can be used to adjust all 3 upper signals simultaneously, and can be considered the part's output amplitude control.

Further signal shaping can take place in the data output buffer DOB using control signals vddshD, and xadjp/xadjn. Pin vddshD can improve the quality of the output eye by

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increasing/decreasing under/overshoot. Differential analog control voltage xadjp/xadjn can be utilized to adjust the crossing points of single-ended output eyes. At the default state of xadjp = xadjn = 0*V*, the crossing points in both direct and inverted eyes should be centered. The crossing points are moving up in the direct eye and down in the inverted eye if xadjp = -xadjn > 0, or in the opposite directions if xadjp = -xadjn < 0.

The part's I/Os support CML logic interface with on-chip 50*Ohm* termination to ground. External 50*Ohm* termination is also required, and is usually provided by the adjacent IC or when testing measurement instrumentation is used. DC-coupling for the data output ports is strongly recommended. The input ports can use DC or AC coupling. Differential input clock, and data are strongly recommended.

TERMINAL FUNCTIONS

TERMINAL			Description
Name	**No.**	**Type**	
High-Speed I/Os			
d1p	32	CML Inputs	Differential high-speed data inputs
d1n	30		
d2p	6		Differential high-speed data inputs
d2n	4		
ci0p	39		Differential high-speed clock inputs
ci0n	41		
qp	19	CML Outputs	Differential high-speed data outputs (PAM4)
qn	17		
Analog Control Voltage Inputs			
xadjp	28	Analog Inputs with 100*kohm* termination to vcc	Output data eye cross point adjustment, differential
xadjn	26		
tune1	8		Analog control amplitude adjustment MSB, SE
tune2	10		Analog control amplitude adjustment LSB, SE
vth	15		Threshold voltage for the analog control maximum value adjustment
dlyadj	37		Adjustment of Delay 2 blocks, SE
skwadj	43		Adjustment of Delay 1 blocks, SE

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply	1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply	2, 13, 24, 35
vddshD	Output data peaking adjustment	21

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POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.6*V*), or a positive supply (vcc = +3.6*V* and vee = 0.0*V*=ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = +3.6*V* and vee = 0*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Power Supply Voltage (vcc)		4.0	*V*
Power Consumption		1.36	*W*
RF Input Voltage Swing (SE)		1.2	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	3.4	3.6	3.8	*V*	
vee		0.0		*V*	External ground
Power		1.25		*W*	
Junction temperature	0	50	100	*°C*	
Data inputs (dp/dn)					
Rate	1.0		26.5	*Gb/s*	
SE Swing	50	200	500	*mV*	Peak-to-peak
CM Level		vcc-(SE swing)/2			
Clock input (ci0p/ci0n)					
Frequency	1.0		26.5	*GHz*	Any skwadj and dlyadj
SE Swing	50	200	500	*mV*	Peak-to-peak
CM Level		vcc-(SE swing)/2			
Data output (qp/qn)					
Rate	2.0		53	*Gbps*	
SE Swing	0.0		1250	*mV*	Peak-to-peak
CM Level	vcc-0.1		vcc-0.75	*V*	Depends on the amplitude
Rise/Fall Times	12	13	14	*ps*	20%-80%
SE tuning ports (tune1, tune2, skwadj, dlyadj)					
Linear control voltage	vcc-2		vcc	*V*	
Switch-off threshold		vcc-2		*V*	
Cross point control (xadjp/xadjn)					
Differential voltage range	vcc-8.0		vcc+8.0	*V*	±4*V* at each input
CM Level		vcc			
Current in/out of the pin		+4 / -4		*mA*	at +4*V* / -4*V*
Threshold control (vth)					
Voltage range	vcc-2		vcc	*V*	
Externally Controlled Operational Ranges					
Clock-to-Clock skew	-30		+30	*ps*	skwadj control
Clock and Data delay	0		+45	*ps*	dlyadj control
Output eye cross point	-25		+25	*%*	of the eye amplitude
Variable supply voltages (vddshD)					
Voltage range	2.8		3.6	*V*	

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PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package. The dimensioned drawings are shown in Fig. 2. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6101-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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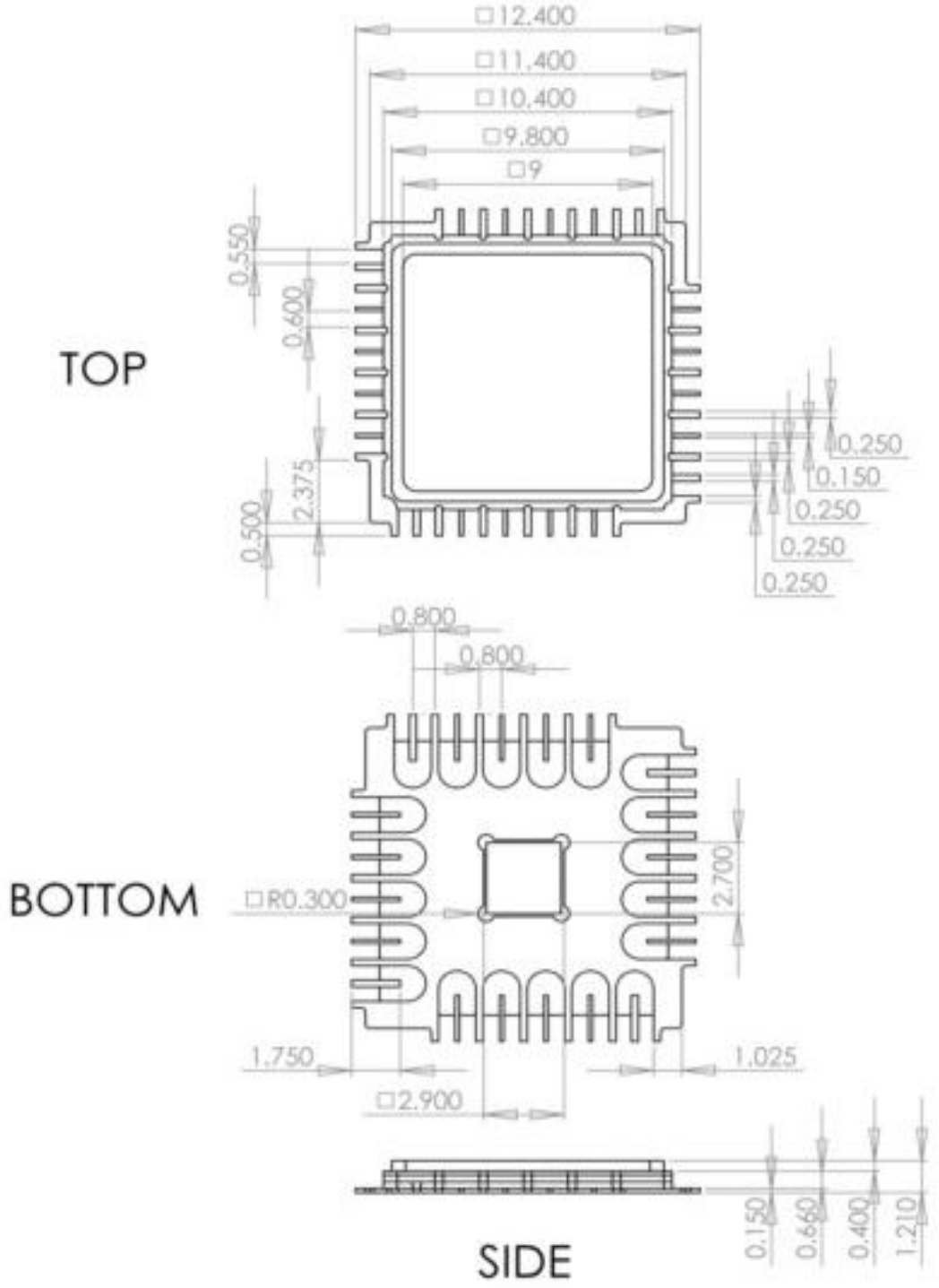

Fig. 2. CQFP 44-Pin Package Drawing (All Dimensions in mm)

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REVISION HISTORY

Revision	Date	Changes
1.2.2	02-2020	Updated Package Information
1.1.2	07-2019	Updated Letterhead
1.1.1	10-2016	Updated title specifications Updated electrical characteristics
1.0.1	01-2016	First release