

Ultra High-Speed Mixed Signal ASICs

Offices: 310-530-9400 / Fax: 310-530-9402 www.adsantec.com

ASNT6901-MOD 64*Gbaud* PAM4 Data Generator with USB Control

- Adjustable data output amplitude and eye quality
- Output data eye cross point adjustment
- Built-in 4-chanel phase-aligned programmable PRBS7-PRBS31 data generator
- Programmable custom data pattern with up to 1*Mbit* length
- Internal precision low jitter (below 1ps p-p) frequency synthesizer
- Alternate external reference clock input
- Differential CML PAM4 data output interface
- Can be used as a PRBS Data Generator up to 64*Gbaud*
- Reference clock-divided-by-2 output
- Precision delay adjustment on clock input
- USB port for connection to an external PC
- Full functional control from GUI software
- Single +12*V* power supply from an external AC-DC converter
- High speed 1.85mm connectors for PAM4 differential data output
- Low jitter and limited temperature variation over industrial temperature range



Fig. 1. Front and Back Views of the Unit



DESCRIPTION

The ADSANTEC's differential PAM4 generator unit can be used for test applications, design verification, and R&D environments. The PAM4 Generator can also be configured to operate as a PRBS or custom word NRZ generator. The fully self-sustained device is integrated in a box with power conditioning, control circuitry, and a USB computer interface. All signal I/O's are CML-type. The front panel of the instrument is shown in Fig. 1 (top). It includes connectors as described in Table 1.

Table 1. Front-Panel Connectors

| Connector | | DESCRIPTION | | | | |
|-----------------|----------------|--|--|--|--|--|
| Name | Type | | | | | |
| High-Speed I/Os | | | | | | |
| PAM4 DATA OUT P | 1.85 <i>mm</i> | DC-coupled CML differential data output port, requires external SE | | | | |
| PAM4 DATA OUT N | female | 50 <i>Ohm</i> terminations to ground | | | | |
| CLOCK IN P | 2.92mm | AC-coupled CML SE clock input port with internal SE 500hm | | | | |
| | female | terminations to ground | | | | |
| CLOCK OUT | CMA | AC-coupled CML SE clock output ports, require external SE 500hm | | | | |
| TRG | SMA | terminations to ground | | | | |

The back panel of the instrument is shown in Fig. 1 (bottom). It contains a power switch (Power), a power supply female connector (+9-12V DC) for connecting a male 2.5x5.5 barrel jack from an external AC-DC adapter, and a USB-B connector (USB) for connecting an external PC with installed Windows GUI control software.

The PAM4 generator's functional block diagram is shown in Fig. 2.

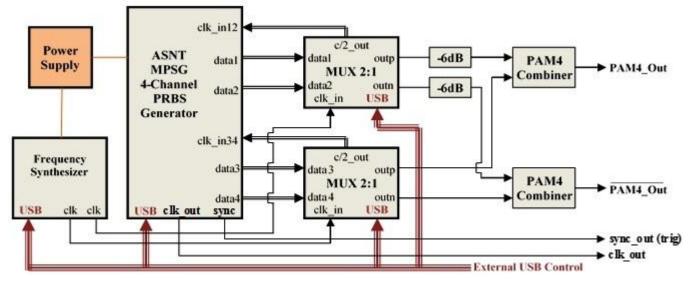


Fig. 2. Block Diagram of 1-Channel PRBS PAM4 Generator

The system consists of five main parts: a Frequency Synthesizer, a Four-Channel PRBS Generator, two high-speed 2:1 Multiplexers, two high-speed differential PAM4 combiners, and a Power Supply unit. The Frequency Synthesizer generates internal clock signals that are used by other parts of the system. It also generates a synchronization signal (not shown in the diagram) as a divided down clock with a Rev. 1.3.2 July 2019 2



ELECTRICAL CHARACTERISTICS

Offices: 310-530-9400 / Fax: 310-530-9402 www.adsantec.com

selectable division ratio from 4 to 1024 at multiples of 2. This signal can be used to trigger an outside oscilloscope.

The Four-Channel PRBS Generator delivers four user-defined binary signals. The signals may be programmed as PRBS7-PRBS31 patterns with pre-defined initial states, or as a custom data pattern with up to 1.0*Mbit* length. The four output signals are phase-aligned, and two pairs of signals are processed by two 2:1 MUXes to produce two PRBS signals with doubled data rate. The MUXes also provide the clock required for the Four-Channel PRBS Generator. The clock phases may be individually adjusted in each MUX2:1 module via the USB control interface.

The output signals from 2:1 MUXes are mixed in two PAM4 combiners to form a differential PAM4 signal. The output amplitude of this signal may be adjusted. The amplitude of the middle eye opening can be individually adjusted without affecting the top and bottom eye opening amplitudes. Alternatively, the system may be programmed to output PRBS data or a custom word pattern instead of PAM4 data through the same I/Os.

All the parameters of this PAM4 Generator are controlled by an external PC through a USB port. A special GUI software is installed on the PC to simplify the system control.

| PARAMETER | TYPICAL | UNIT | COMMENT | | | |
|------------------------|-----------------------|-------------|---|--|--|--|
| General Parameters | | | | | | |
| Vcch | 12 | V | Power Supply | | | |
| Vccm | 5 | V | Internal Power Supply | | | |
| Vccl | 3.3 | V | Internal Power Supply | | | |
| Vee | 0 | V | External Ground | | | |
| Power Consumption | 133 | W | | | | |
| | Inp | ut Internal | Clock | | | |
| Frequency | 0.5-32 | GHz | From Frequency Synthesizer | | | |
| Jitter | 1 | ps | | | | |
| _ | | Output Da | ta | | | |
| Data Rate | 1-64 | Gbaud | | | | |
| Maximum Output | 1.2 | V | Differential pk-pk | | | |
| Amplitude | | | | | | |
| Rise / Fall Time | 8 | ps | 80%-20% | | | |
| TDECQ (no FFE) | 1.5 | dB | With Rx Optimizer | | | |
| TDECQ (with 5-tap FFE) | 1.2 | dB | With Rx Optimizer | | | |
| Output Clock | | | | | | |
| Frequency | 0.25-16 | GHz | Internal Clock divided by 2 | | | |
| | Output Sync (Trigger) | | | | | |
| | | | Internal Clock divided by selectable division | | | |
| Frequency | 0.0005-16 | GHz | ratio from 2 to 1024 at multiples of 2 | | | |

Table 2. PAM4 Generator Specifications

Offices: 310-530-9400 / Fax: 310-530-9402 www.adsantec.com

MECHANICAL DIMENSIONS

The Unit's external dimensions are presented in Table 3.

| Table 3. | Unit's External Dimensions |
|----------|----------------------------|
|----------|----------------------------|

| PARAMETER | TYP | UNIT | COMMENTS |
|-----------|-----|------|----------|
| Length | TBD | mm | |
| Width | TBD | mm | |
| Height | TBD | mm | |

REVISION HISTORY

| Revision | Date | Changes | |
|----------|---------|--|--|
| 1.3.2 | 07-2019 | Updated Letterhead | |
| 1.3.1 | 05-2018 | Updated Mechanical Dimensions section | |
| | | Format adjustments | |
| 1.2.1 | 05-2018 | Updated rise/fall time in Electrical Characteristics | |
| 1.1.1 | 01-2018 | Corrected title | |
| | | Corrected description | |
| | | Added Table with connector descriptions | |
| 1.0.1 | 11-2017 | Initial Release | |





Offices: 310-530-9400 / Fax: 310-530-9402 www.adsantec.com

Ultra High-Speed Mixed Signal ASICs