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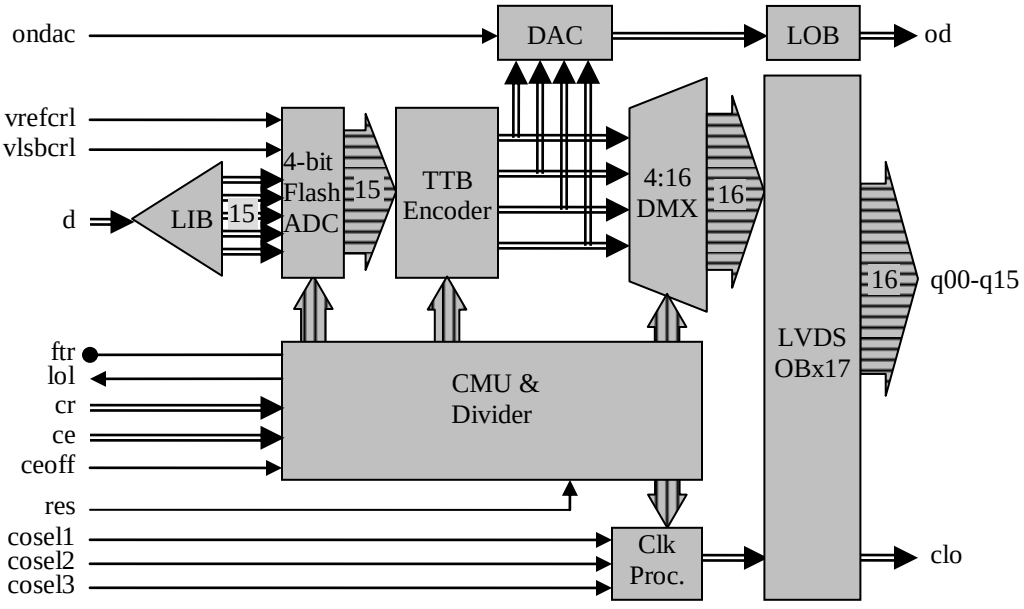
ASNT7120-KMA
10*GS/s*, 4-bit Flash Analog-to-Digital Converter

- 18*GHz* analog input bandwidth.
- Selectable clocking mode: external high-speed clock or internal PLL with external low-speed reference clock.
- Broadband operation in external clocking mode: DC-10*GS/s*.
- On-chip PLL with a central frequency of 10*GHz*.
- Optional external preset of the internal clock divider.
- Internal demultiplexer 4-to-16 for the output data rate reduction.
- Fully differential input data and clock buffers with on-chip 50*Ohm* termination.
- Proprietary low-power LVDS output interface.
- Selectable output clock frequency and polarity.
- Selectable on-chip digital-to-analog converter for self-testing.
- Single +3.5*V* power supply.
- Power consumption: 2.4*W*.
- Custom 100-pin metal-ceramic package.



Functional Block Diagram

DESCRIPTION

The ASNT7120-KMA is a 10*GS/s* 4-bit flash analog to digital converter (ADC) featuring 18*GHz* of analog front-end bandwidth. The ADC system includes a linear input buffer (LIB) with a tree architecture and CML-type input interface with internal 50*Ohm* single-ended terminations to "vcc". The buffer delivers 15 matching copies of the input analog data signal ("d") to the 4-bit flash ADC. The ADC creates 15 samples of the input data in thermometer code, which are then converted into 4-bit binary words with a data rate of 10*Gb/s*. The encoded data is demultiplexed into 16-bit wide words with a data rate of 2.*5Gb/s* and sent to the output through 16 low-power LVDS buffers. An optional digital-to-analog converter (DAC) can be used for the control of the ADC's operation.

All operations are synchronized by the internal clock multiplication unit (CMU) based on PLL (phase-locked loop) with an integrated divider. The block can operate in two different modes: clock multiplication (PLL is on) and clock division (PLL is off). In both modes, the divider generates internal clock signals divided by 2, 4, 8, and 16. The generated clocks divided by 4, 8, and 16 are sent to the LVDS output ("clo") through a clock processor that selects the desired speed ("cosel1", "cosel2" control signals) and polarity ("cosel3" control signal) of the output clock. In the second operational mode of CMU, the divider can be preset by the external signal ("res") to ensure the correct phase relation between the output data and clock.

The part operates from a single +3.5V power supply. All external control signals are compatible with the 2.5*V* CMOS interface.

Linear Input Buffer (LIB)

The system includes a linear input buffer (LIB) with a tree-type architecture that delivers 15 matching copies of the input differential analog data signal ("dp"/"dn") with up to 18*GHz* of analog bandwidth to the 4-bit flash section. Symmetry is closely followed in both schematic and layout to ensure minimal aperture jitter.

Clock Multiplication Unit (CMU) & Divider

The PLL-based CMU with external loop filter connected to pin ("ftr") can operate in two different modes. In the first "clock multiplication" mode ("ceoff"=1), CMU multiplies the external 625*MHz* reference clock ("crp"/"crn") by means of PLL with a central frequency of 10*GHz* and the tuning range of the internal VCO (voltage-controlled oscillator) from 9.0*GHz* to 11.0*GHz*.

The generated clock is processed by the divider in order to generate internal clock signals divided by 2, 4, 8, and 16. In the second "clock division" mode ("ceoff"=0), PLL is disabled and the internal clocks are generated from the external high-speed clock ("cep"/"cen"). To ensure correct bit order, the divider can be present by the active-high CMOS control signal ("res"). A special control signal "cpcsel" can be used to fine-tune the PLL loop gain. It is recommended for the users to keep this pin not-connected (at default state).

4-bit Flash Analog to Digital Converter (ADC) with Encoder

This block samples the incoming analog data with the clock signal provided by CMU in order to generate a 4-bit output digital signal with MSB corresponding to Bit 0. Threshold voltages (V_{th}) of the flash ADS can be adjusted through analog signals "vrefcrl" and "vlsbcrl" as shown in Table 1.

Table 1. Threshold Adjustment Options.

Control signal		Adjusted value	
Name	Range	Name	Range
vrefcrl	2.6*V* -> 3.6*V*	$V_{th\ 15}$	3.42*V* -> 3.05*V*
vlsbcrl	2.8*V* -> 3.4*V*	$V_{th\ (X+1)} - V_{th\ X}$	560*uV* -> 59*mV*

As can be seen, "vrefcrl" shifts the DC levels of all the threshold voltages simultaneously by the same amount while "vlsbcrl" alters the voltage range of the least significant bit (LSB).

Demultiplexer (4:16 DMX)

This block deserializes the 4-bit words from ADC into 16-bit output words. The LSB bit 0 is represented by data outputs from "q00" to "q03", while the MSB bit 3 is represented by data outputs "q12" to "q15".

Clock Processor (Clk Proc)

To increase the adaptability of the designed ADC, a clock processor that provides a low-speed output clock signal with the options specified in Table 2, is included.

Table 2. Output Clock Options.

External control signals			Output clock signal	
"cosel1"	"cosel2"	"cosel3"	Speed	Inversion
0	0	0	c4	Yes
0	0	1	c4	No
x	1	0	c8	Yes
x	1	1	c8	No
1	0	0	c16	Yes
1	0	1	c16	No

Digital to Analog Converter (DAC)

A DAC block is included to perform a quick test of the ADC's functionality. When activated by the external control signal ("ondac"="1"), it converts the digital data into a step-wise copy of the input signal that is sent to the output ("odp"/"odn") through a linear differential output buffer. The circuit is not consuming any power when disabled ("ondac"="0").

LVDS Output Buffers

The 16-bit differential digital data words ("qXXp"/"qXXn") are delivered to the output through an array of proprietary low power LVDS buffers. The low speed differential clock ("clop"/"clon") also utilizes a similar LVDS output buffer.

TERMINAL FUNCTIONS

Pin #	Pin name	Pin type	Pin #	Pin name	Pin type	Pin #	Pin name	Pin type
1	vee	GND	35	vcc	3.5V	69	q12p	LVDS outputs
2	vee	GND	36	vee	GND	70	q12n	
3	q02p	LVDS outputs	37	vee	GND	71	vcc	3.5V
4	q02n		38	vcc	3.5V	72	q11p	LVDS outputs
5	vcc	3.5V	39	dn	HS CML inputs	73	q11n	
6	q01p	LVDS outputs	40	dp		74	vee	GND
7	q01n		41	vcc	3.5V	75	vee	GND
8	vcc	3.5V	42	vee	GND	76	vcc	3.5V
9	q00p	LVDS outputs	43	vee	GND	77	q10p	LVDS outputs
10	q00n		44	vcc	3.5V	78	q10n	
11	vcc	3.5V	45	n/c		79	vcc	3.5V
12	clop	LVDS outputs	46	res	CMOS input	80	q09p	LVDS outputs
13	clon		47	ondac	CMOS input	81	q09n	
14	n/c		48	vlsbcrl	Control voltages	82	vcc	3.5V
15	vee	GND	49	vrefcrl		83	q08p	LVDS outputs
16	cosel1	CMOS input	50	vee	GND	84	q08n	
17	cosel2	CMOS input	51	vee	GND	85	vcc	3.5V
18	cosel3	CMOS input	52	n/c		86	q07p	LVDS outputs
19	lol	Control output	53	n/c		87	q07n	
20	ftr	Filter	54	n/c		88	vcc	3.5V
21	vee	GND	55	vcc	3.5V	89	q06p	LVDS outputs
22	ceoff	CMOS input	56	odp	LS CML outputs	90	q06n	
23	vee	GND	57	odn		91	vcc	3.5V
24	cpcsel	CMOS input	58	vee	GND	92	q05p	LVDS outputs
25	vcc	3.5V	59	n/c		93	q05n	
26	vcc	3.5V	60	q15p	LVDS outputs	94	vcc	3.5V
27	crn	LVDS inputs	61	q15n		95	q04p	LVDS outputs
28	crp		62	vcc	3.5V	96	q04n	
29	vcc	3.5V	63	q14p	LVDS outputs	97	vcc	3.5V
30	vee	GND	64	q14n		98	q03p	LVDS outputs
31	vee	GND	65	vcc	3.5V	99	q03n	
32	vcc	3.5V	66	q13p	LVDS outputs	100	vcc	3.5V
33	cen	HS CML inputs	67	q13n				
34	cep		68	vcc	3.5V			

vee – negative supply voltage (ground)
vcc – positive supply voltage

cep – high-speed lines (15GHz)
clop – low-speed lines (1GHz)
ceoff – control signals (DC)
ftr – external PLL filter

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE		0.0		V	
VCC	3.4	3.5	3.6	V	±3%
IEE		680		mA	
Power		2.4		W	
Junction Temp.	-25	50	125	°C	
Data Input (ADin)					
Bandwidth	0.0		18	GHz	
CM Level	"vcc"-0.8		"vcc"	V	
Linearity range		±110		mV	Around CM level
Non-linearity		±3		%	of the range
HS Clock Input (ce)					
Bandwidth	0.0		10	GHz	
CM Level	"vcc"-0.8		"vcc"	V	
Voltage Swing	100		800	mV	Differential
Ref. Clock Input (cref)					
Bandwidth	600		700	MHz	
CM Level	0		"vcc"	V	
Voltage Swing	100		800	mV	Around CM level
Data Output (q)					
Data rate	0.0		2.5	Gbps	
CM Level*		1.2		V	
Amplitude range	250		350	mV	
Rise/Fall Times		TBD		ps	20%-80%
Clock Output (clo)					Selectable, where
Clock frequency		F/4, F/8, F/16			F is PLL frequency
CM Level*		1.2		V	
Amplitude range	250		350	mV	
DAC Output (daco)					
Voltage Swing	250		350	mV	Single-ended
CM Level	"vcc"- 1/2 voltage swing			V	
Controls (vrfcrl/vlsbcrl)					
Voltage Range	"vcc"-0.5		"vcc"	mV	Single-ended
CMOS Controls					
Low level	0		0.2	V	
High level	2.3		2.5	V	

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings presented in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 3. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Supply Voltage - VCC		-4.0	*V*
Power Consumption		2.75	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Operational Temperature	-5	+85	*ºC*
Case Temperature		+100	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

PACKAGE INFORMATION

The chip die is housed in a custom, 100-pin metal-ceramic quad flat package (CQFP). The package dimensioned drawings are included in this document for reference. The package leads will be trimmed to a length of 1.0mm.

After trimming, the package leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal

2. The leads will be tinned with Sn63Pb37 solder.

It is recommended that the center heat slug located on the back side of the package *not* be soldered to ground or any other potential to help dissipate heat generated by the chip during operation. For PCB information including footprint etc., please reference the package's associated Gerber file.

The part's identification label is ASNT7120_KMA. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

For ASNT7120_KMA:

- ASNT7120 identifies that the part is a 4-bit flash ADC
- K represents the fact that it is a Kyocera package
- M stands for metal ceramic
- A means that the package has 100 pins

A date is included in the label of each part. This date allows ADSANTEC to track which parts are from which run lot. The table below gives the lot history of this part and the associated date.

Lot	Date
1	04/10

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.2 Previous release Rev 1.1 1-2011	6-2011	Added Absolute Maximums Rating table Added packaging information Added RoHS compliancy Added revision history table