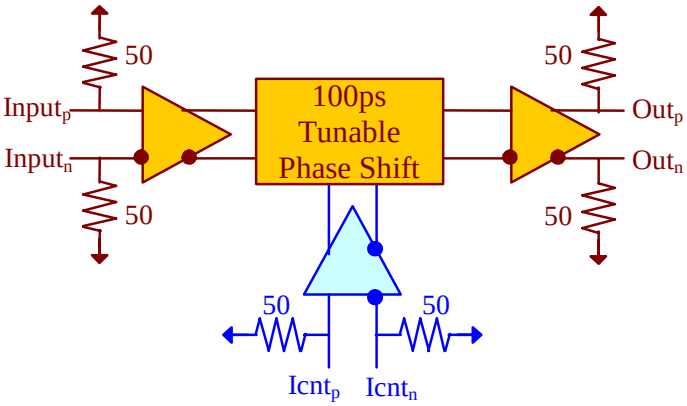
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

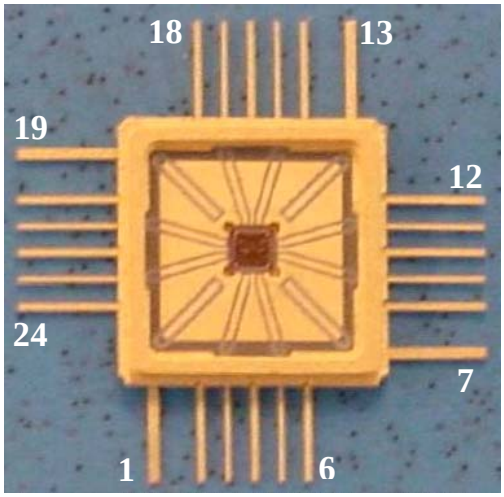
ASNT5102-KMC
32*GHz* Phase Shifter

- Broadband (10*MHz*-32*GHz*/20*Mbps*-60*Gbps*) tunable clock/data phase shifter with 100*ps* of delay variation.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 1G*Hz* of bandwidth for the phase adjustment tuning port.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 1050*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT5102-KMC SiGe IC provides a broadband signal phase shifting capability between its input and output signal ports and is intended for use in high-speed measurement / test equipment. ASNT5102-KMC can process an up to 32*GHz*/50*Gbps* RF clock/data signal and deliver 0-100*ps* of adjustable phase delay through the up to 1*GHz* external adjustment of its differential tuning port. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3*V* power supply.

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TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL (NO.)	TYPE	DESCRIPTION
vcc	2,4,6,8,10,12 14-18,20,22,24	PS	Power Supply: 3.3V / 0V
vee	1,7,13,19	PS	Power Supply: 0V / -3.3V
inp	21	Input	Differential CML high-speed signal inputs
inn	23		
outp	11	Output	Differential CML high-speed signal outputs
outn	9		
icntp	3	Input	Differential low-speed phase adjustment tuning inputs
icntn	5		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		320		mA	
Power		1050		mW	
Junction Temp.	-25	50	125	°C	
Input (in)					
Frequency	0.0		32/60	GHz/Gbps	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
SE Swing	50	400	1000	mV	Peak-to-Peak
Output (out)					
Frequency	0.0		32/60	GHz/Gbps	
CM Level	Vcc-0.3	Vcc-0.33	Vcc-0.35	V	
SE Swing		400		mV	Peak-to-Peak
Rise/Fall Times	9	10	11	ps	20%-80%
Additive Jitter		TBD		ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal
Tuning Port (icnt)					
Diff. Swing	-500		500	mV	Peak-to-Peak
CM Level	Vcc-0.5	Vcc-0.25	Vcc	V	
Phase Shift	0		100	ps	
Shift Stability	-3		3	ps	0-125°C
Bandwidth	0.0		1000	MHz	

PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's website.