ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

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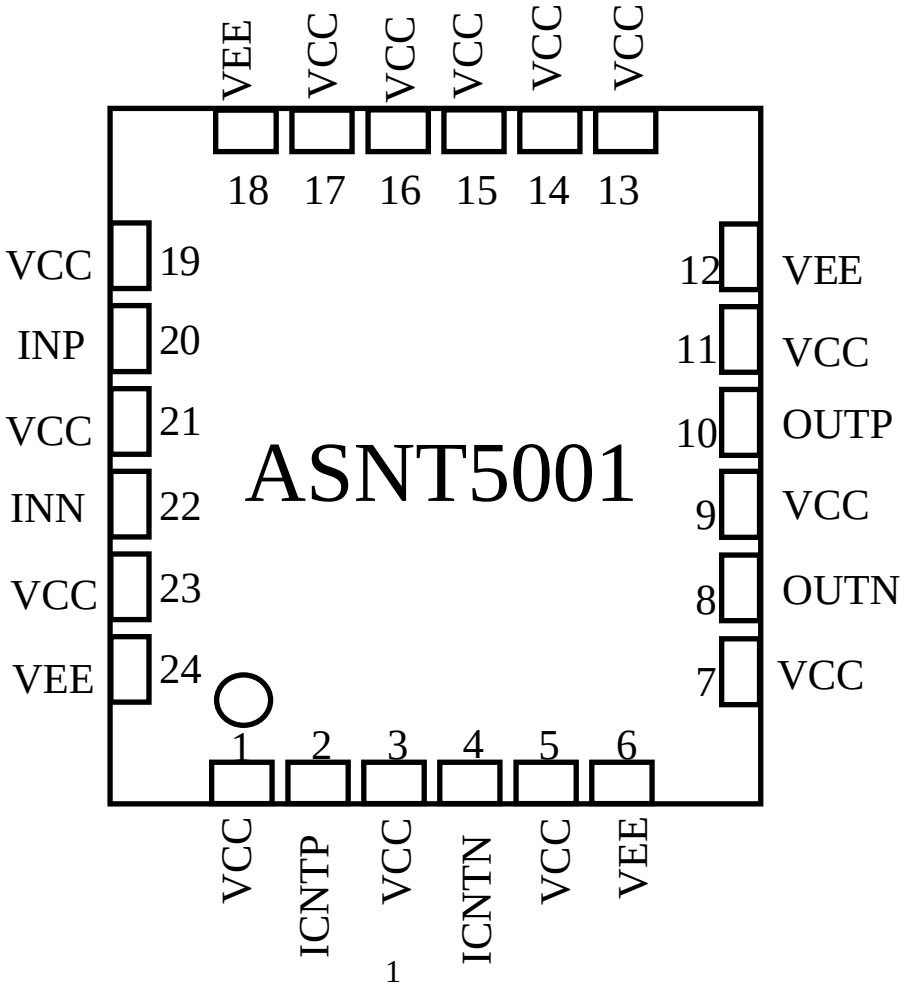
ASNT5001-PQC
17*GHz* Clock or 28*Gbps* Data Phase Shifter with Linearized OB

- Broadband (10*MHz*-17*GHz* / 20*Mbps*-28*Gbps*) tunable clock/data phase shifter.
- Delay adjustment range of 250*ps*.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 1*GHz* of bandwidth for the phase adjustment tuning port.
- Fully differential CML input interface.
- Fully differential CML output interface with 600*mV* single-ended swing.
- Linearized data output for minimized undershoot/overshoot.
- Single +3.3*V* or -3.3*V* power supply.
- Power consumption: 1.15*W*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



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DESCRIPTION

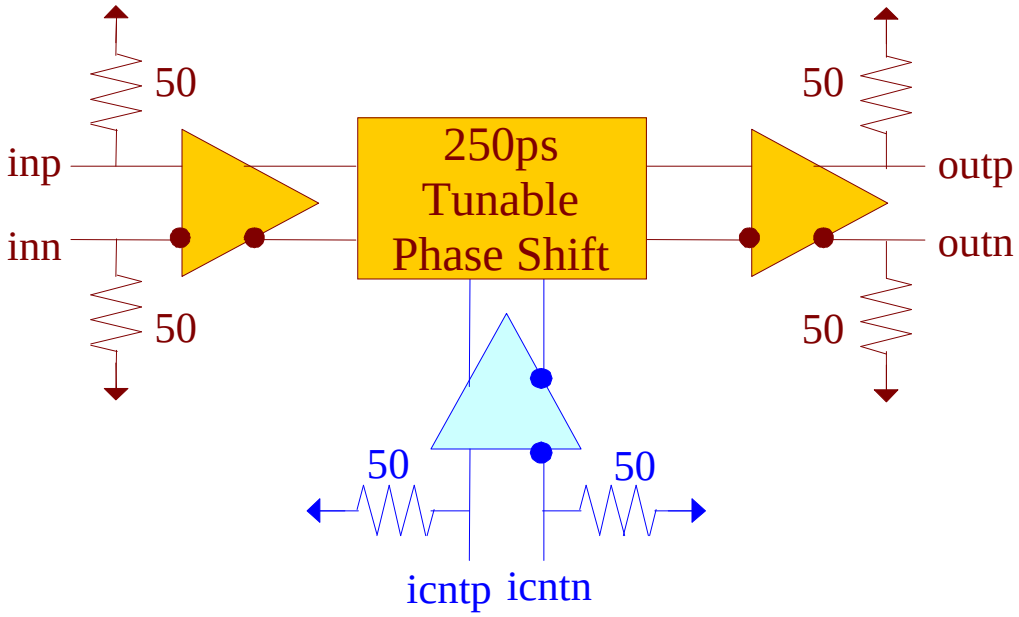

Fig. 1. Functional Block Diagram

ASNT5001-PQC is a clock / data variable delay line fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of a broadband signal applied to its input port ("inp/inn"), with a temperature-stabilized adjustment range. Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment. The part's I/Os support the CML logic interface with on chip 50*Ohm* termination to "vcc" and may be used differentially, AC/DC coupled, single-ended, or in any combination. The delay is controlled through a wide-band differential tuning port ("icntp/icntn"). The delay control diagram is shown in Fig. 2. The output buffer is linearized for reduction of undershoots and overshoots on the output waveforms.

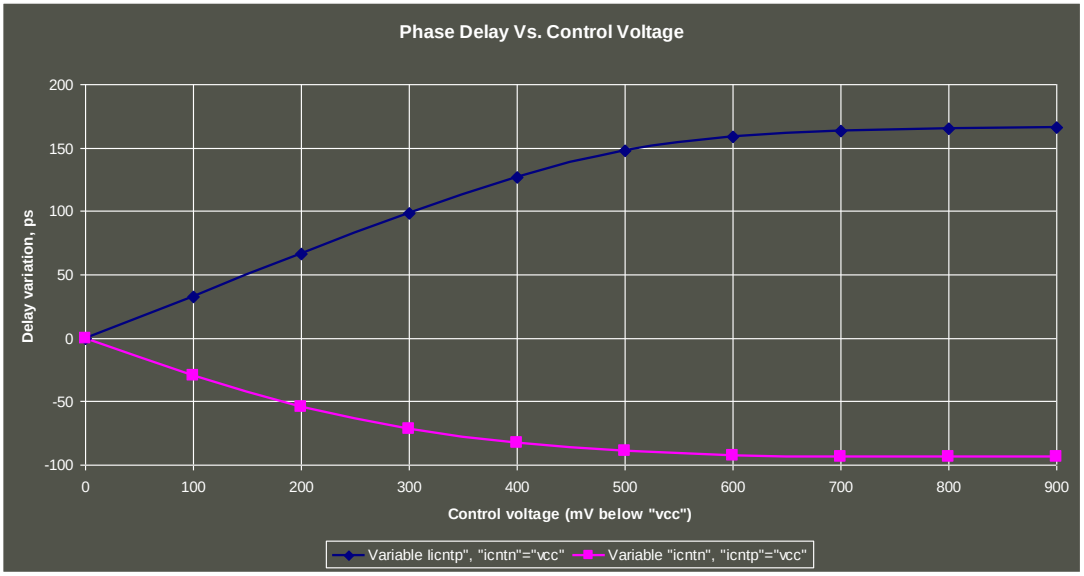

Fig. 2. Delay Control Diagram.

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POWER SUPPLY CONFIGURATION

The ASNT5001-PQC can operate with either a negative supply ("vcc" = 0.0*V*=ground and "vee" = -3.3*V*), or a positive supply ("vcc" = +3.3*V* and "vee" = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume "vcc" = 0.0*V* and "vee" = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed "vcc").

Table 1. Absolute Maximum Ratings.

Parameter	Min	Max	Units
Supply Voltage ("vee")		-3.6	*V*
Power Consumption		0.5	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL (NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11 13-17,19,21,23	PS	Positive power supply or ground
vee	6,12,18,24	PS	Ground or negative power supply
inp	20	Input	Differential CML high-speed signal inputs
inn	22		
outp	10	Output	Differential CML high-speed signal outputs
outn	8		
icntp	2	Input	Differential wide-band phase adjustment tuning signal inputs
icntn	4		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
Ivee		350		*mA*	
Power		1.15		*W*	
Junction Temp.	-25	50	125	*°C*	
Input (in) Data rate/Clock frequency	0.0		28/17	*Gbps/GHz*	
SE Swing	50	400	1000	*mV*	Peak-to-Peak
CM Level	"vcc"-(SE swing)/2			*V*	
Output (out) Data rate/Clock frequency	0.0		28/17	*Gbps/GHz*	
SE Swing	570	600	630	*mV*	Peak-to-Peak
CM Level	"vcc"-(SE swing)/2			*V*	
Phase Shift	0		250	*ps*	< ±5%
Shift Stability	-4		2	*ps*	0-125°C
Rise/Fall Times	15	17	19	*ps*	20%-80%
Additive Jitter		TBD		*ps*	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal
Tuning Port (icnt) SE voltage level	"vcc"-1000		"vcc"	*mV*	When the opposite pin is at "vcc"
SE swing	0		1000	*mV*	Peak-to-Peak in differential mode
CM Level	"vcc"-(SE swing)/2			*V*	In differential mode
Bandwidth	0.0		1000	*MHz*	

PACKAGE INFORMATION

The chip die is housed in a standard 24-pin QFN package shown in Fig. 3. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part's identification label is ASNT5001-PQC. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

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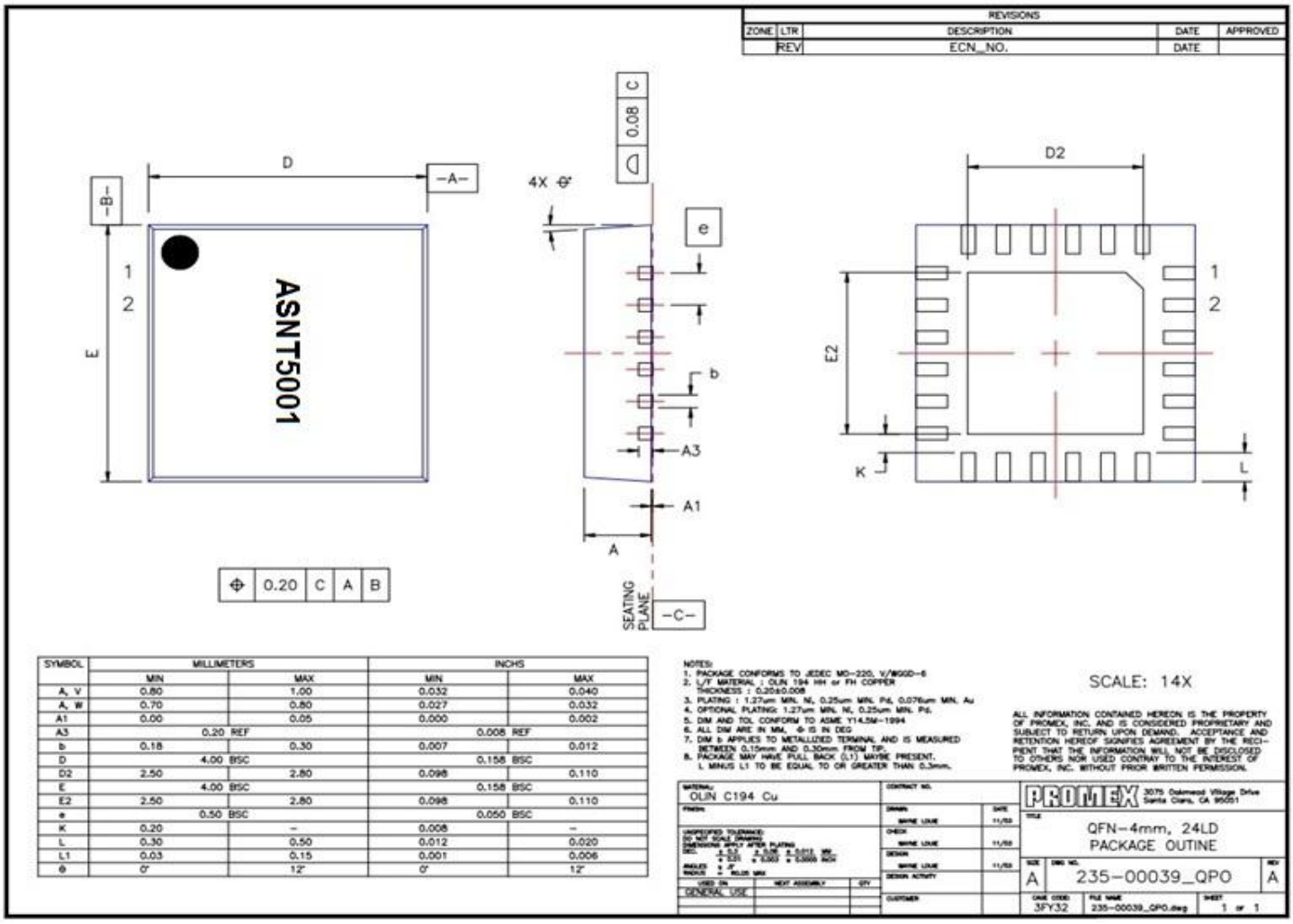

SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A, V	0.80	1.00	0.032	0.040
A, W	0.70	0.80	0.027	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.00 BSC		0.158 BSC	
D2	2.50	2.80	0.098	0.110
E	4.00 BSC		0.158 BSC	
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.050 BSC	
K	0.20	–	0.008	–
L	0.30	0.50	0.012	0.020
L1	0.03	0.15	0.001	0.006
θ	0°	12°	0°	12°

Fig. 3. Package Drawing.

REVISION HISTORY

Revision	Date	Changes
1.4	2-2012	Revised Description section Revised Power Supply Configuration section
1.3	1-2012	Added absolute maximum ratings table Added power supply recommendations table Added mechanical drawing of package
1.2	12-2011	Modified electrical characteristics table Modified title and description Added revision history table
1.1	9-2011	Initial Release