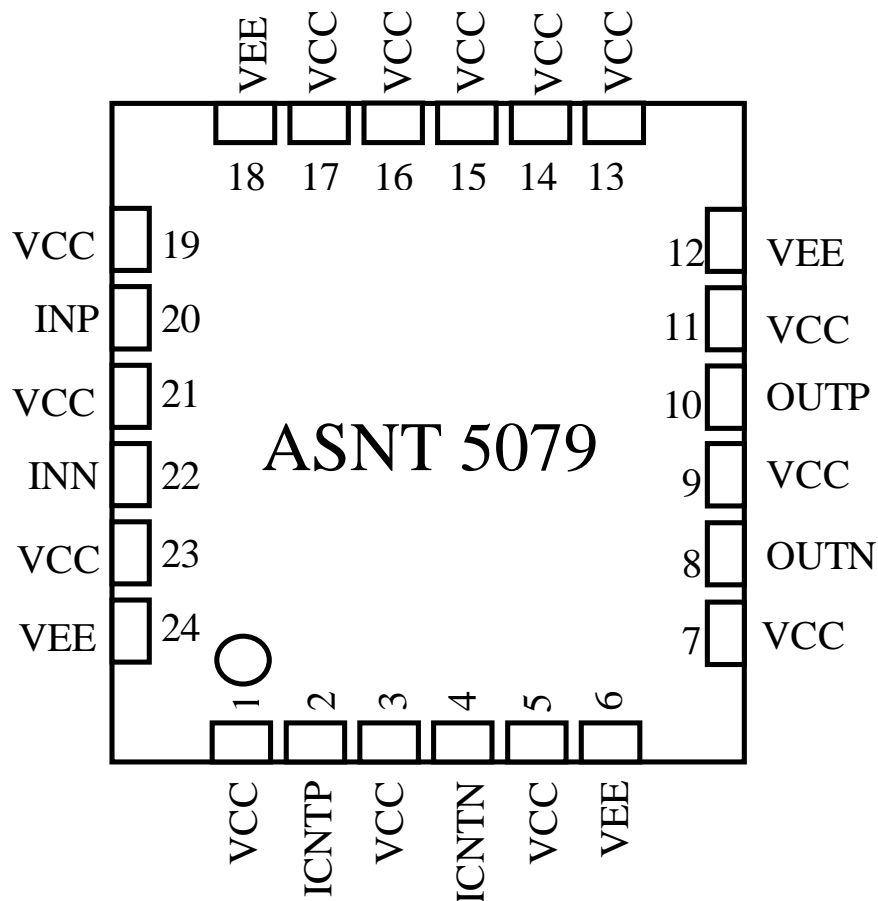


ASNT5079-PQC

14GHz Clock, 17Gbps Data Phase Shifter with Linear OB

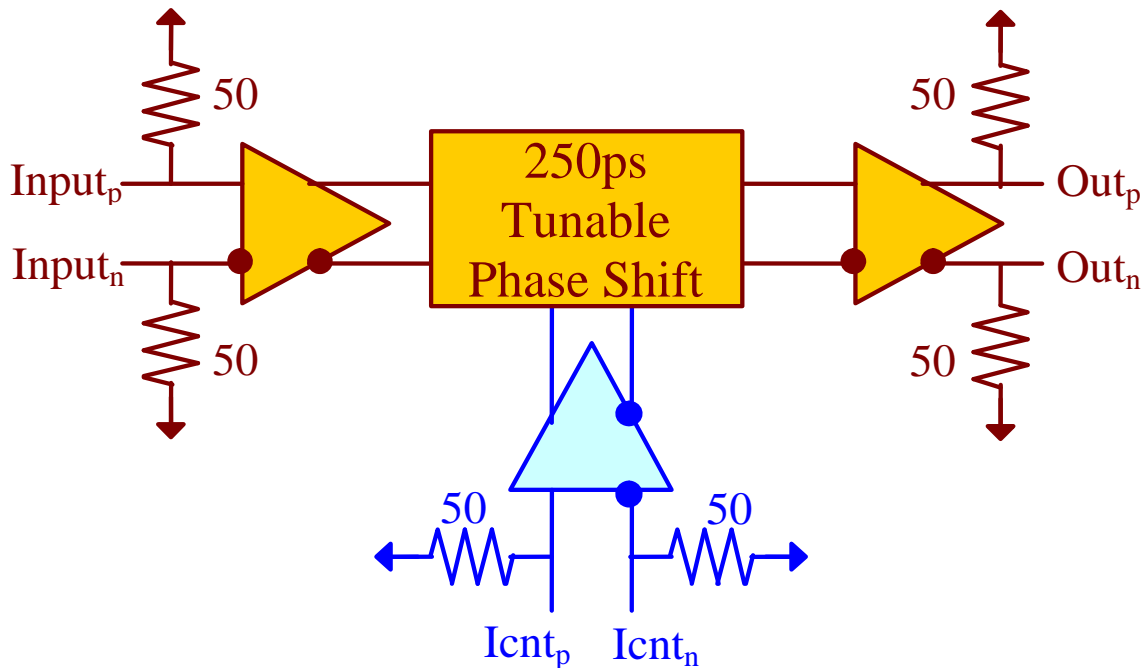
- Broadband (10MHz-14GHz/20Mbps-17Gbps) tunable clock/data phase shifter with 250ps of delay variation.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 1GHz of bandwidth for the phase adjustment tuning port.
- Fully differential input and output buffers with on-chip 50Ω termination.
- Linearized data output for minimized undershoot/overshoot.
- CML output interface with 600mV single-ended swing.
- Single ±3.3V power supply.
- Power consumption: 1.6W.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



DESCRIPTION

The temperature stable ASNT5079-PQC SiGe IC provides extremely low jitter broadband signal phase shifting capability between its input and output signal ports and is intended for use in high-speed measurement / test equipment. ASNT5079-PQC can process an up to 14GHz/17Gbps RF clock/data signal and deliver 0-250ps of adjustable phase delay through the up to 1GHz external adjustment of its differential tuning port. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. The output buffer is linearized for reduction of undershoot and overshoot. The part operates from a single ±3.3V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11 13-17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
inp	20	Input	Differential CML high-speed signal inputs
inn	22	Input	
outp	10	Output	Differential CML high-speed signal outputs
outn	8	Output	
icntp	2	Input	Differential low-speed phase adjustment tuning inputs
icntn	4	Input	



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE	450	475	500	mA	
Power		1.6		W	
Junction Temp.	-25	50	125	°C	
Input (in)					
Data rate/Clock frequency	0.0		17/14	Gbps/GHz	
CM Level	V _{cc} -0.8	V _{cc} -0.2	V _{cc}	V	
SE Swing	50	400	1000	mV	Peak-to-Peak
Output (out)					
Data rate/Clock frequency	0.0		17/14	Gbps/GHz	
CM Level	V _{cc} -0.35	V _{cc} -0.3	V _{cc} -0.25	V	
SE Swing	570	600	630	mV	Peak-to-Peak
Rise/Fall Times	15	17	19	ps	20%-80%
Additive Jitter		TBD		ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal
Tuning Port (icnt)					
Diff. Swing	-500		500	mV	Peak-to-Peak
CM Level	V _{cc} -0.5	V _{cc} -0.25	V _{cc}	V	
Phase Shift	0		250	ps	< ±5%
Shift Stability	-24		24	ps	0-125°C
Bandwidth	0.0		1000	MHz	

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's [website](#).