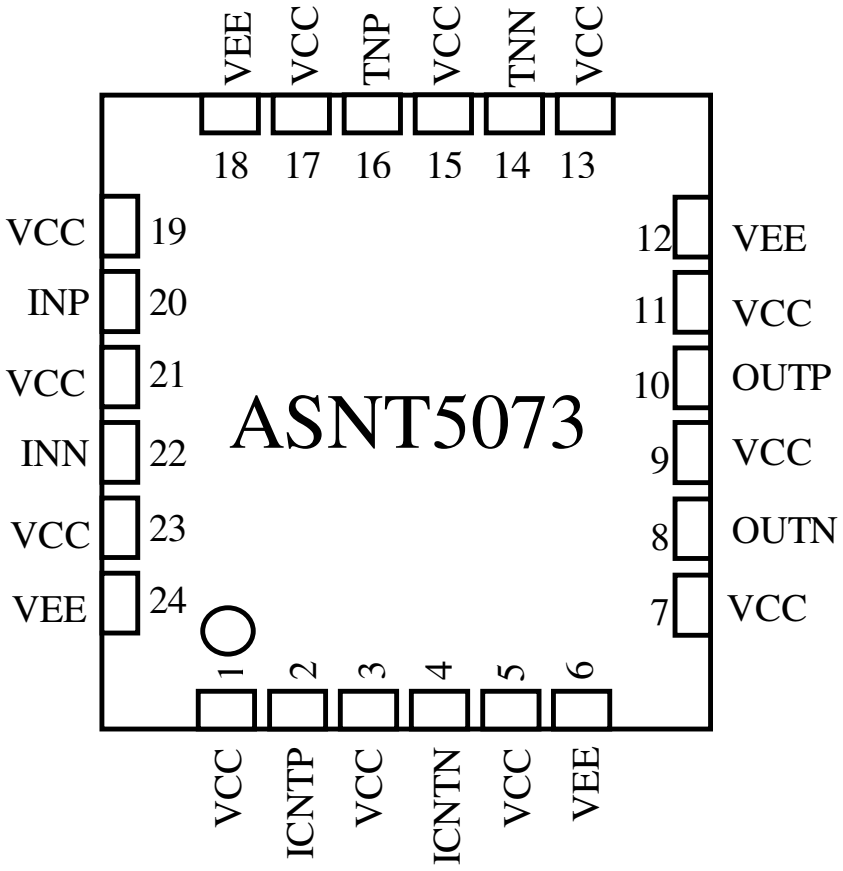
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5073-PQC
14*GHz* Clock, *17Gbps* Data Phase Shifter with Output Signal Amplitude Control

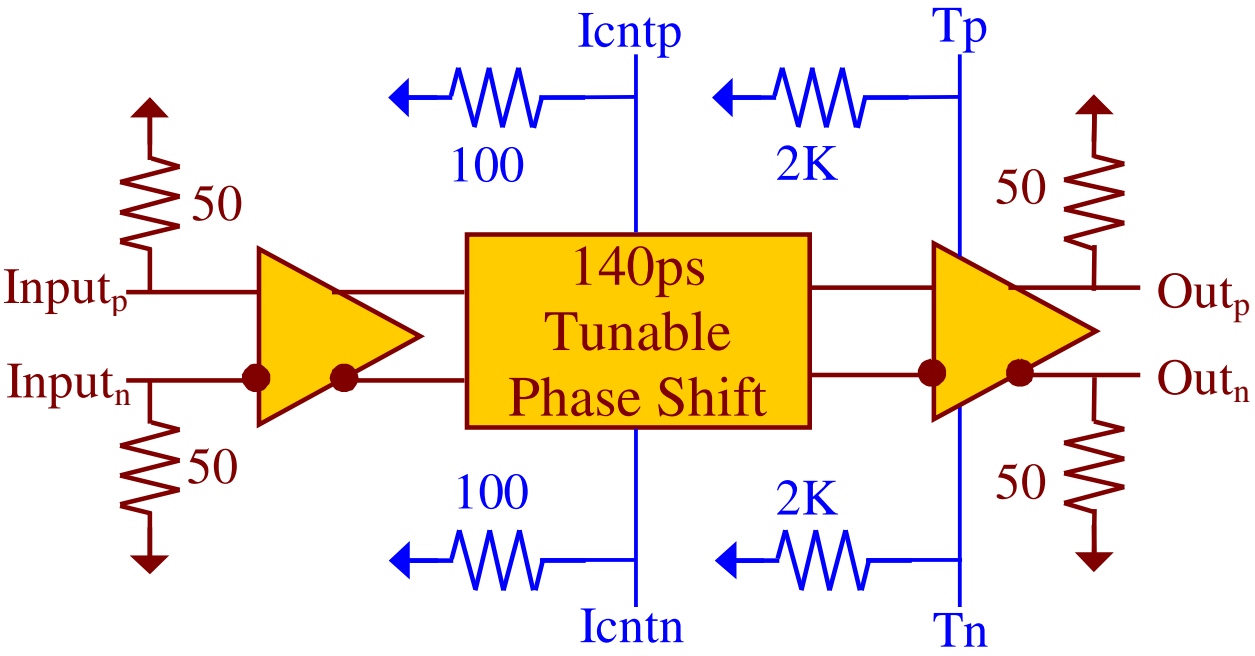
- Broadband (DC-14*GHz*/DC-17*Gbps*) tunable clock/data phase shifter with 140*ps* of delay variation.
- Output signal amplitude adjustment from 0.0*V* to 0.8*V* single ended.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 100*MHz* of bandwidth for the phase adjustment tuning ports.
- 10*MHz* of bandwidth for the amplitude adjustment tuning ports.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- Single ±3.3*V* power supply.
- Power consumption: 1.1*W*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



DESCRIPTION

The temperature stable ASNT5073-PQC SiGe IC provides extremely low jitter broadband signal phase shifting and amplitude control capability between its input and output signal ports and is intended for use in high-speed measurement / test equipment. ASNT5073-PQC can process an up to 14*GHz*/17*Gbps* RF clock/data signal and deliver both 0-140*ps* of adjustable phase delay and output signal amplitudes between 0.0*V*-0.8*V* through two external adjustment differential tuning ports. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11 13,15,17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
inp	20	Input	Differential CML high-speed signal inputs
inn	22		
outp	10	Output	Differential CML high-speed signal outputs
outn	8		
icntp	2	Input	Differential low-speed phase adjustment tuning inputs
icntn	4		
tnp	16	Input	Differential low-speed amplitude adjustment tuning inputs
tnn	14		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		330		mA	
Power		1.1		W	
Junction Temp.	-25	50	125	°C	
Input (in)					
Frequency	0.0		17/14	Gbps/GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
Swing (Diff or SE)	50	400	1000	mV	Peak-to-Peak
Output (out)					
Frequency	0.0		17/14	Gbps/GHz	
CM Level*	Vcc-0.25	Vcc-0.2	Vcc-0.15	V	
SE Swing*	380	400	420	mV	Peak-to-Peak
Amplitude Variation	0.0	400	800	mV	
Rise/Fall Times*	15	17	19	ps	20%-80%
Additive Jitter		4		ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal
Tuning Port (icnt)					
Diff. Swing	-500		500	mV	Peak-to-Peak
CM Level	Vcc-0.5	Vcc-0.25	Vcc	V	
Phase Shift Control	0		140	ps	
Shift Stability	-12		12	ps	0-125°C
Bandwidth	0.0		100	MHz	
Tuning Port (tn)					
Diff. Swing	-500		500	mV	Peak-to-Peak
CM Level	Vcc-0.5	Vcc-0.25	Vcc	V	
Bandwidth	0.0		100	MHz	
* Tn pins are not connected (NC)					

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.