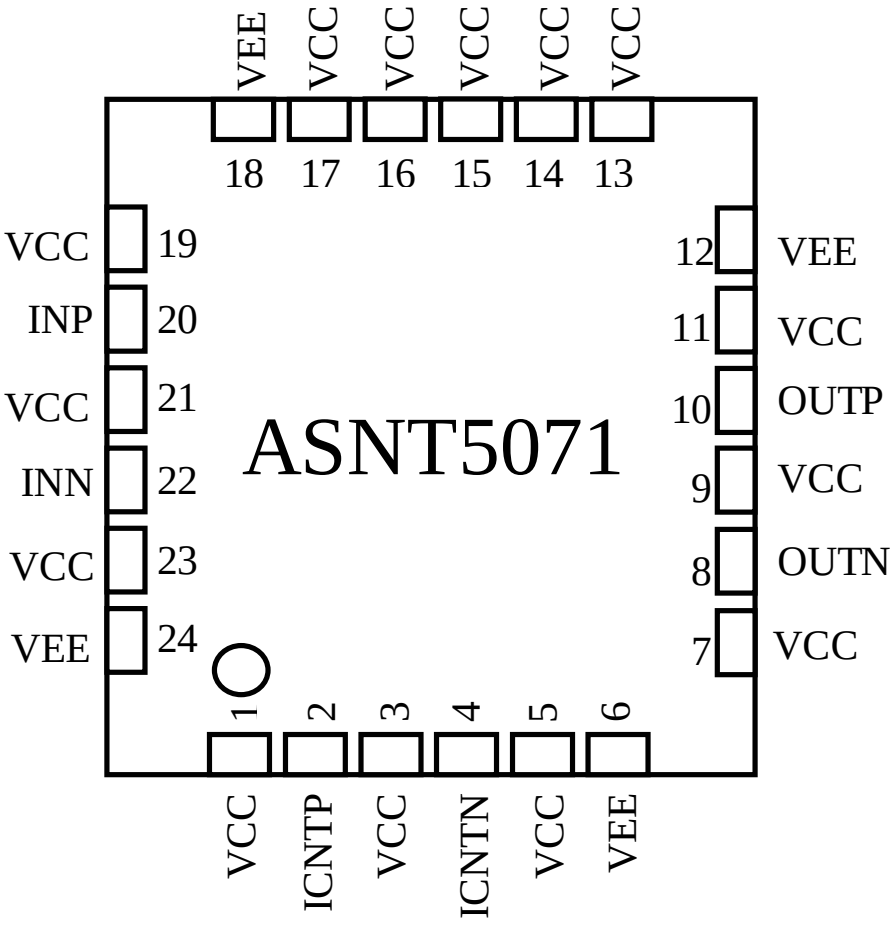
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5071-PQC
10*GHz* Clock, 17*Gbps* Data Phase Shifter

- Broadband (10*MHz*-10*GHz*/20*Mbps*-17*Gbps*) tunable clock/data phase shifter with 320*ps* of delay variation.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 100*MHz* of bandwidth for the phase adjustment tuning port.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 600*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 1.44*W*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



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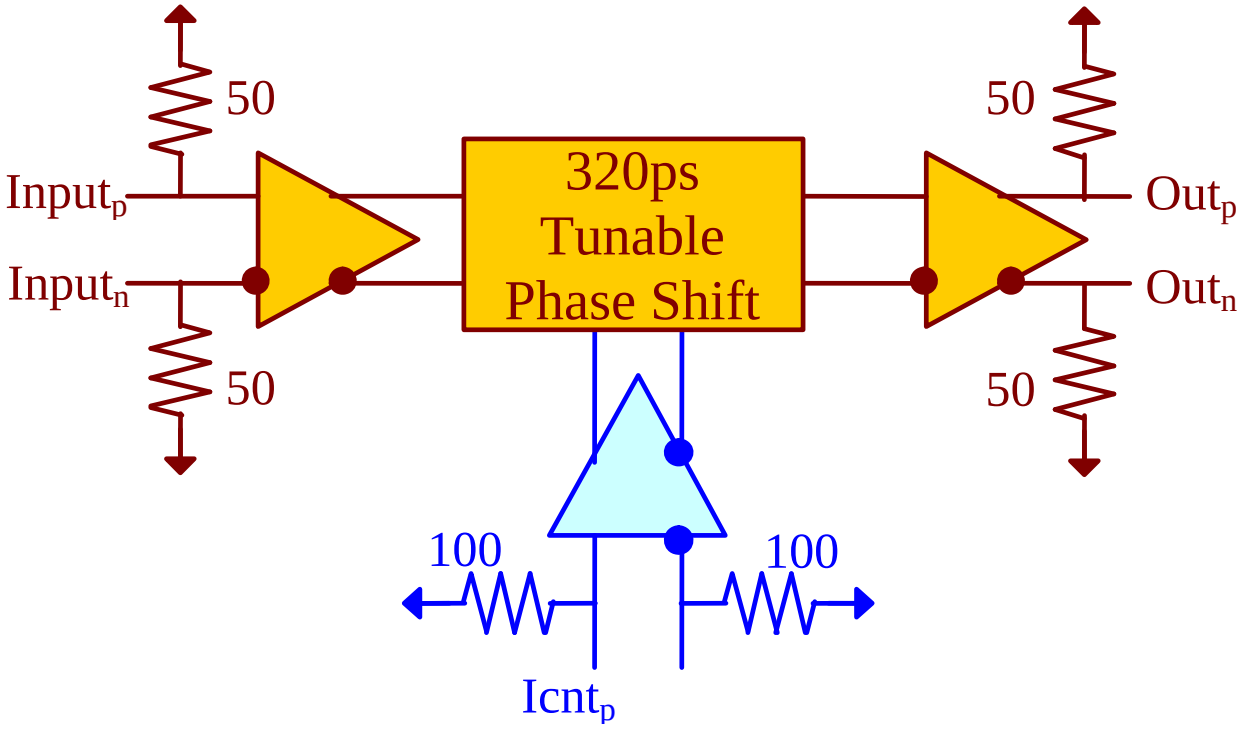
DESCRIPTION

The temperature stable ASNT5071-PQC SiGe IC provides extremely low jitter broadband signal phase shifting capability between its input and output signal ports and is intended for use in high-speed measurement / test equipment. ASNT5071-PQC can process an up to 10*GHz*-17*Gbps* clock/data signal and deliver 0-320*ps* of adjustable phase delay through the up to 100*MHz* external adjustment of its differential tuning port. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3*V* power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	(NO.)		
vcc	1,3,5,7,9,11 13-17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
inp	20	Input	Differential CML high-speed signal inputs
inn	22		
outp	10	Output	Differential CML high-speed signal outputs
outn	8		
icntp	2	Input	Differential low-speed phase adjustment tuning inputs
icntn	4		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		435		mA	
Power		1.44		W	
Junction Temp.	-25	50	125	°C	
Input (in)					
Data rate/Clock frequency	0.0		17/10	Gbps/GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
Swing (Diff or SE)	50	400	1000	mV	Peak-to-Peak
Output (out)					
Data rate/Clock frequency	0.0		17/10	Gbps/GHz	
CM Level	Vcc-0.35	Vcc-0.3	Vcc-0.25	V	
SE Swing	570	600	630	mV	Peak-to-Peak
Rise/Fall Times	15	17	19	ps	20%-80%
Additive Jitter		TBD		ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal
Tuning Port (icnt)					
Diff. Swing	-500		500	mV	Peak-to-Peak
CM Level	Vcc-0.5	Vcc-0.25	Vcc	V	
Phase Shift Control	0		320	ps	< ±5%
Shift Stability	-30		30	ps	0-125°C
Bandwidth	0.0		100	MHz	

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.