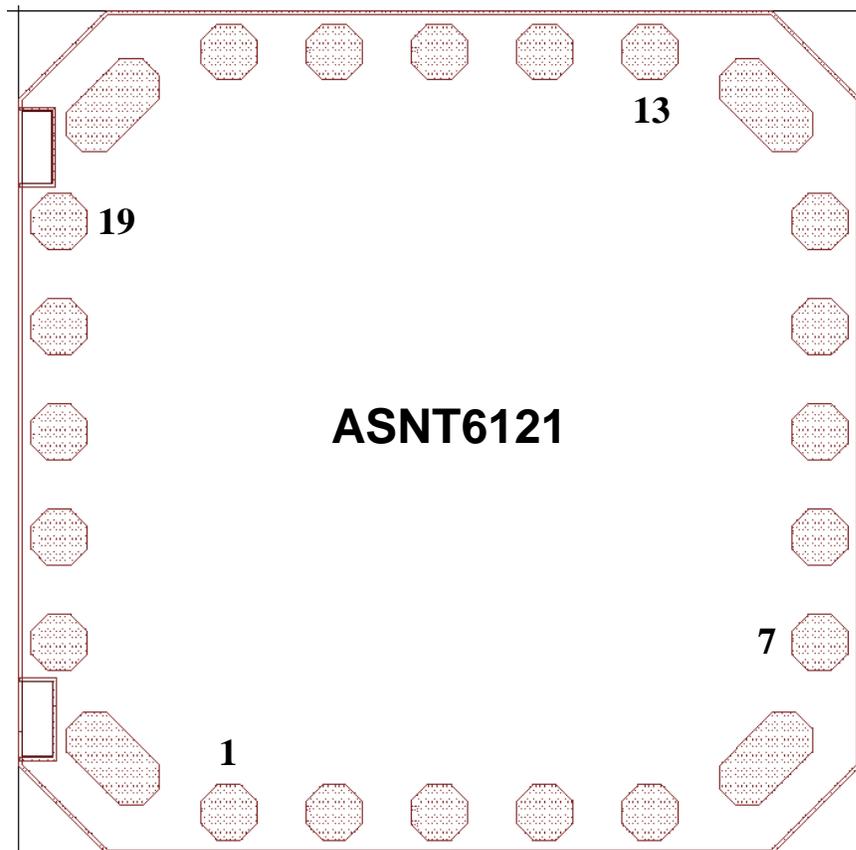




## ASNT6121-BD 45Gbps Linear/Limiting TIA

- Broadband transimpedance amplifier (TIA) for low noise receiver-side applications
- Manual bandwidth/peaking control
- Automatic DC offset adjustment
- Input peak detector
- On-chip temperature detector
- Exhibits low jitter and limited temperature variation over industrial temperature range
- Fully differential output buffer with on-chip  $50\Omega$  termination
- Single +3.3V or -3.3V power supply
- Low current consumption of 145mA at nominal conditions
- Fabricated in SiGe for high performance, yield, and reliability





## DESCRIPTION

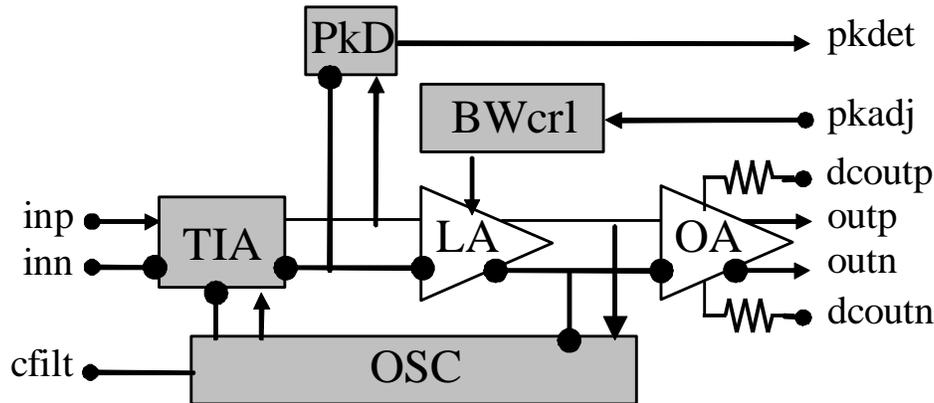


Fig. 1. Functional Block Diagram

The ASNT6121-BD IC is a temperature stable SiGe transimpedance amplifier that provides low-jitter broadband conversion of current signals at its input port **inp** into differential voltage signals at the output ports **outp/outn**. The part shown in Fig. 1 is a serial combination of transimpedance (TIA), limiting (LA), and linearized output (OA) amplification stages. The part operates as a linear amplifier for low input currents and moves to limiting mode above the specified maximum Non-Limiting Current Swing (see ELECTRICAL CHARACTERISTICS). The input signal should be single-ended with the current flowing into the **inp** pin. It is recommended to decouple the **inn** pin to ground with a  $10nF$  capacitor. The part incorporates a control block (BWcr1) with an external port **pkadj** for adjustment of the total bandwidth or peaking of the amplifier, as well as an automatic DC offset control (OSC) that effectively eliminates any difference between the common-mode voltages of direct and inverted output signals. The offset compensation function requires utilization of an external  $100nF$  capacitor attached to the **cfilt** pad. The output common mode voltages on output pins **outp/outn** can be adjusted using analog ports **dcoutp/dcoutn** respectively.

The on-chip peak detector (PkD) provides an output signal **pkdet** proportional to the value of the input signal.

The on-chip temperature sensor is a diode with its anode connected to the **dtemp** port.

The part's outputs support a CML-type interface with on-chip  $50\Omega$  termination and may be used as a differential or single-ended connection with AC or DC-coupling (see also POWER SUPPLY CONFIGURATION). The input and output termination resistors in both channels are respectively connected to separate internal positive supply planes **vcca** and **vccd**. The input and output negative supply nets are also created as separate metal planes **veea** and **veed**, which are partly shorted through the common substrate.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (**vcc** =  $0.0V$  = ground and **vee** =  $-3.3V$ ), or positive supply (**vcc** =  $+3.3V$  and **vee** =  $0.0V$  = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with  $50\Omega$  termination to ground.

The chip substrate should be connected to **vee** or completely isolated. DO NOT connect substrate to **vcc**!



All the characteristics detailed below assume  $V_{CC} = 3.3V$  and  $V_{EE} = 0.0V$ .

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed  $V_{EE}$ ).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage ( $V_{CC}$ )		3.6	V
Power Consumption		0.56	W
RF Input Current Swing (SE)		4	mA
Junction Temperature		+125	$^{\circ}C$
Storage Temperature	-40	+100	$^{\circ}C$
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
inp	20	Current input	Single-ended current-sensing data input
inn	22		Additional input. $10nF$ decoupling to ground is recommended
outp	10	CML output	Differential data outputs. Require external $50\Omega$ termination to $V_{CC}$
outn	8		
<b>Controls</b>			
dcoutp	14	Input	Analog control ports with internal $1K$ terminations to corresponding data outputs outp/outn
dcoutn	4		
pkadj	3	Input	Analog voltage port with internal $2.0K\Omega$ termination to $V_{CC}$
pkdet	15	Output	Analog voltage port with internal $2.8K\Omega$ termination to $V_{CC}$
cfilt	2		$100nF$ off-chip capacitor connection
dtemp	16	Output	Temperature sensor output (sink current)
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vccd	Positive power supply (+3.3V or 0V)		6, 12
vcca	Quiet positive power supply for TIA (+3.3V or 0V)		18, 24
veed	Negative power supply (0V or -3.3V)		5, 7, 9, 11, 13
veea	Quiet negative power supply for TIA (0V or -3.3V)		1, 17, 19, 21, 23



## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vccd	3.1	3.3	3.5	V	±6%
vcca	3.1	3.3	3.5	V	±6%
veed		0.0		V	External ground
veea		0.0		V	External ground
Ivee		145		mA	
Power consumption		480		mW	
Junction temperature	-25	50	125	°C	
<b>HS Input Data (inp/inn)</b>					
Data Rate			45	Gbps	
Bandwidth	16	20	23	GHz	-3dB level
Low Cutoff	2.2		4.4	KHz	-3dB level
Non-Limiting Current Swing			250	uA	pk-pk, positive (into the pin)
Input Overload Current		2.0		mA	
CM Voltage Level	990		1100	mV	Defined by OSC
<b>Output Common Mode Controls (dcoutp, dcoutn)</b>					
Voltage range	vee		vcc	V	For linear DC offset control
<b>Bandwidth Control (pkadj)</b>					
Voltage range	vcc-1.0		vcc	V	
Bandwidth	0		100	MHz	
<b>HS Output Data (outp/outn)</b>					
Data Rate			50	Gbps	
Transimpedance	3.5		5.0	KOhm	Non-saturated output
SE Swing		0.3		V	Peak-to-peak, saturated
CM Level		vcc-(Swing)/2		V	External 50Ohm DC termination
Group Delay Variation		±5		ps	100MHz - 23GHz
Input Referred Noise Density		23		pA/Hz <sup>1/2</sup>	0 - 23GHz
Additive Jitter		1		ps	Peak-to-peak, PRBS7 input
<b>Peak Detector (pkdet)</b>					
Output Voltage range	vcc-1.0		vcc	V	For input current of 80-2000µA



## SIMULATED CHARACTERISTICS

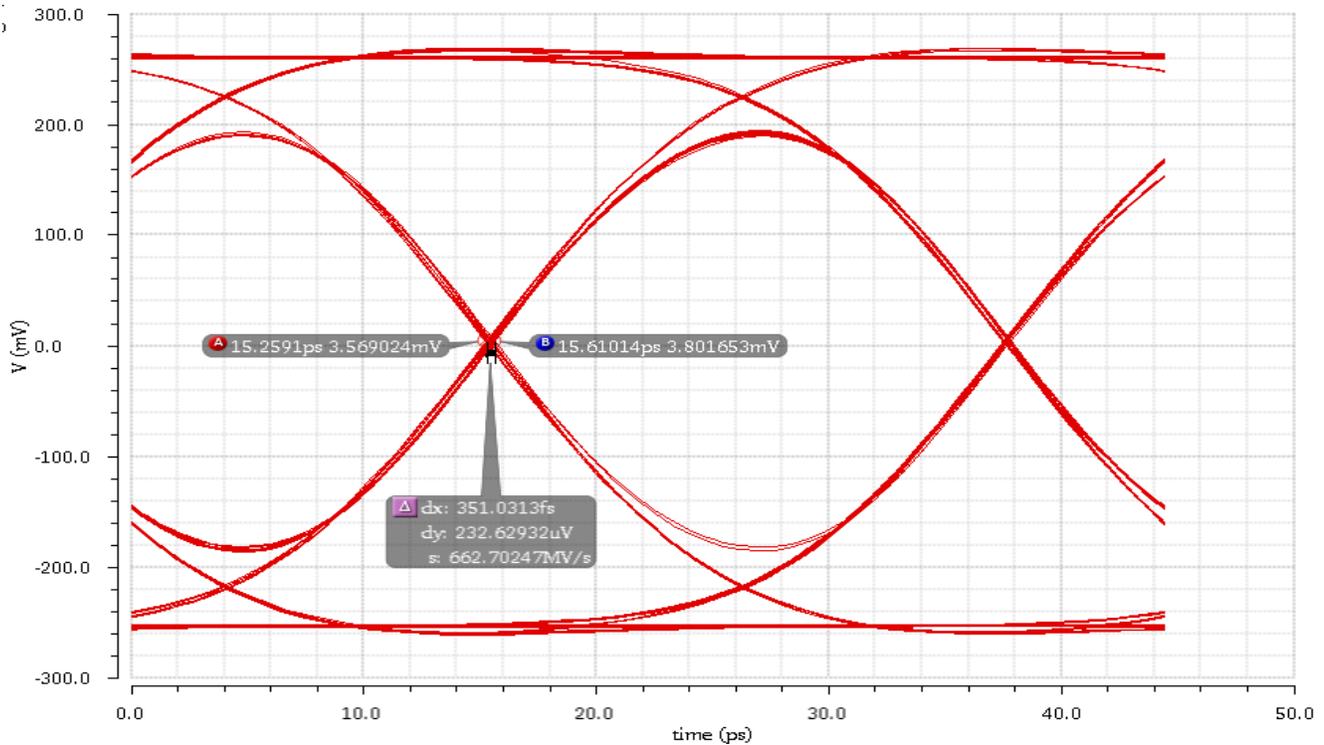


Fig. 2. Typical Output Eye at 200uA Input Current Swing and 45Gbps Data Rate

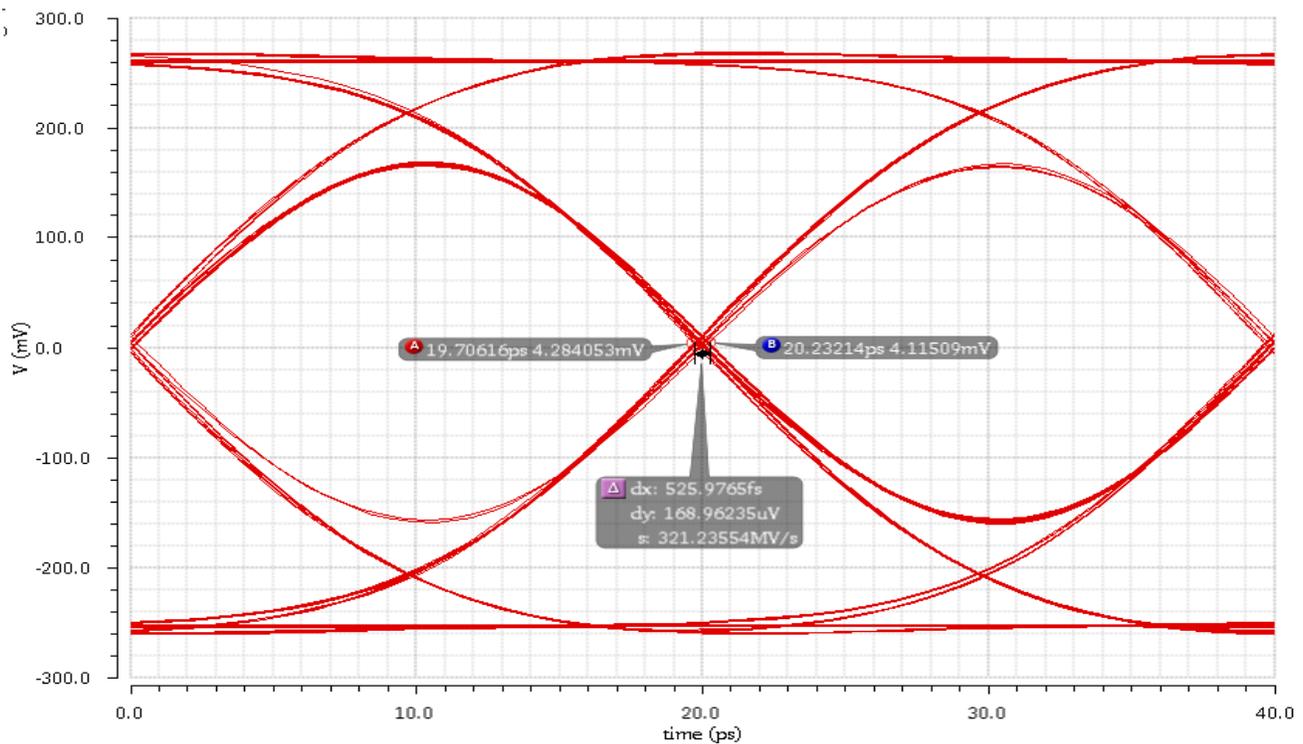


Fig. 3. Typical Output Eye at 200uA Input Current Swing and 50Gbps Data Rate

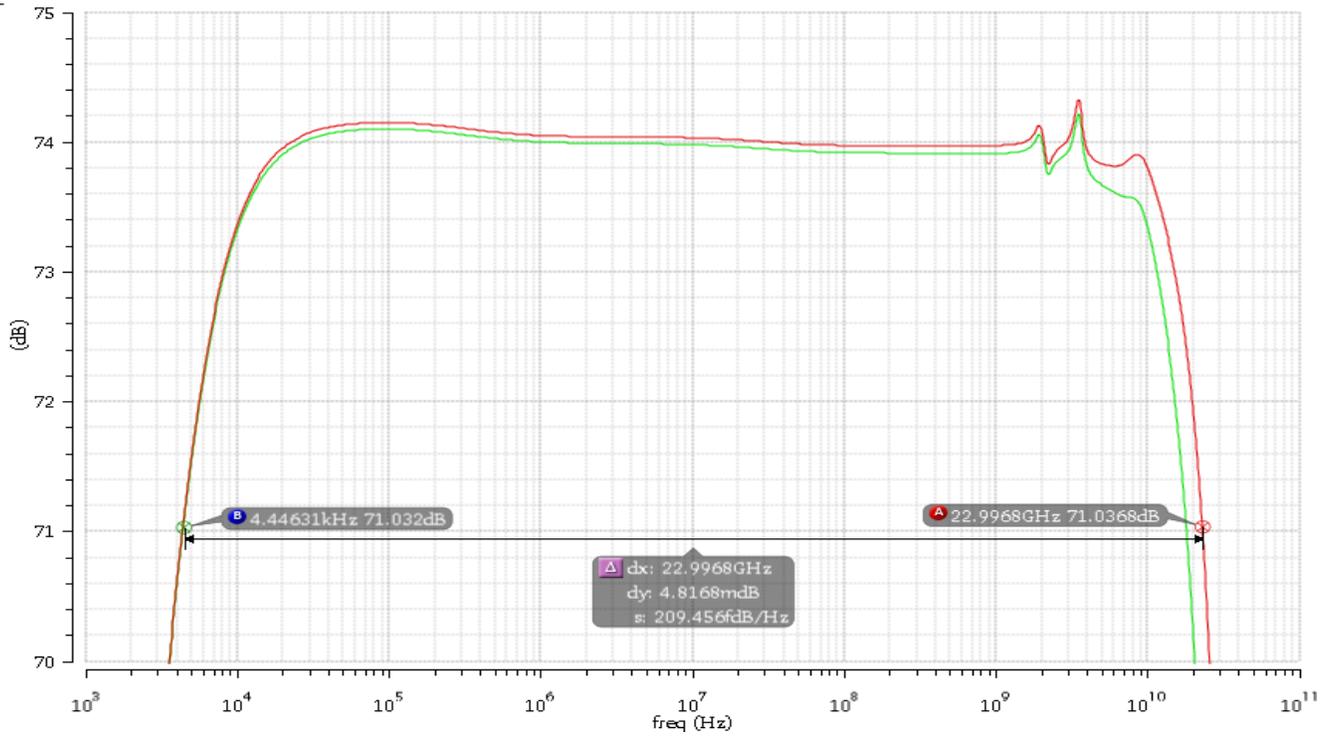


Fig. 4. Typical S21 Characteristic

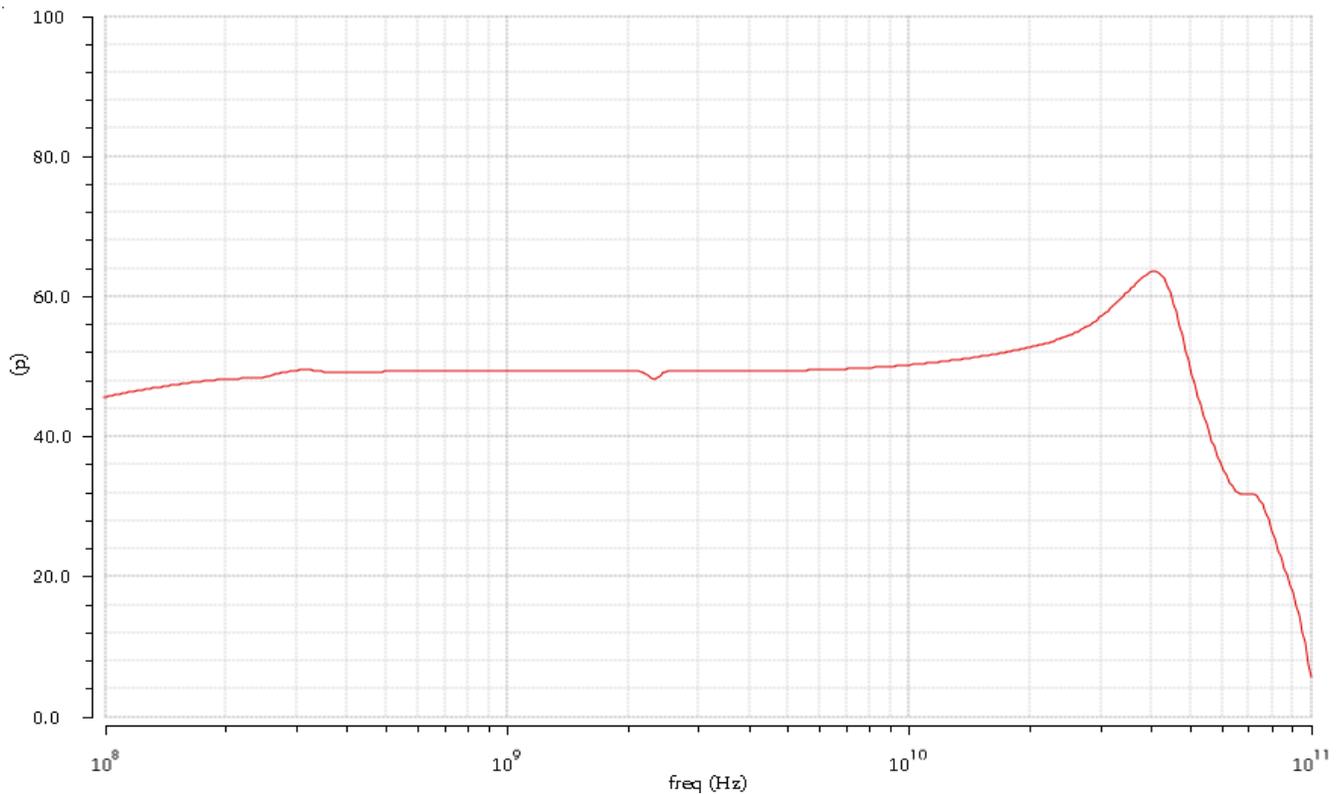


Fig. 5. Typical Group Delay



## DIE INFORMATION

The main dimensions of the die are given in Table 2.

Table 2. Important Die Dimensions

Pad metal dimensions	80 $\mu$ m x 80 $\mu$ m
Pad opening dimensions	74 $\mu$ m x 74 $\mu$ m
Die dimensions	1200 $\mu$ m x 1200 $\mu$ m

The part's die incorporates wire bonding pads with the coordinates of their centers given in Table 3.

Table 3. Die Pad Coordinates

Pin Number	X Coordinate, $\mu$ m	Y Coordinate, $\mu$ m	Pin Number	X Coordinate, $\mu$ m	Y Coordinate, $\mu$ m
1	300	58	2	450	58
3	600	58	4	750	58
5	900	58	6	1065	135
7	1142	300	8	1142	450
9	1142	600	10	1142	750
11	1142	900	12	1065	1065
13	900	1142	14	750	1142
15	600	1142	16	450	1142
17	300	1142	18	135	1065
19	58	900	20	58	750
21	58	600	22	58	450
23	58	300	24	135	135

The part's identification label is ASNT6121-BD. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 2 characters after the dash indicate that the die is not packaged.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



## REVISION HISTORY

Revision	Date	Changes
2.3.2	05-2020	Updated Die Information
2.2.2	07-2019	Updated Letterhead
2.2.1	05-2017	Modified title Corrected description of liner/limiting operational modes
2.1.1	04-2017	Added description of substrate connection Corrected Electrical Characteristics section
2.0.1	02-2017	Fully revised description Added power supply configuration Added absolute maximum ratings Added simulated characteristics Added die information Updated format
1	02-2010	Preliminary release