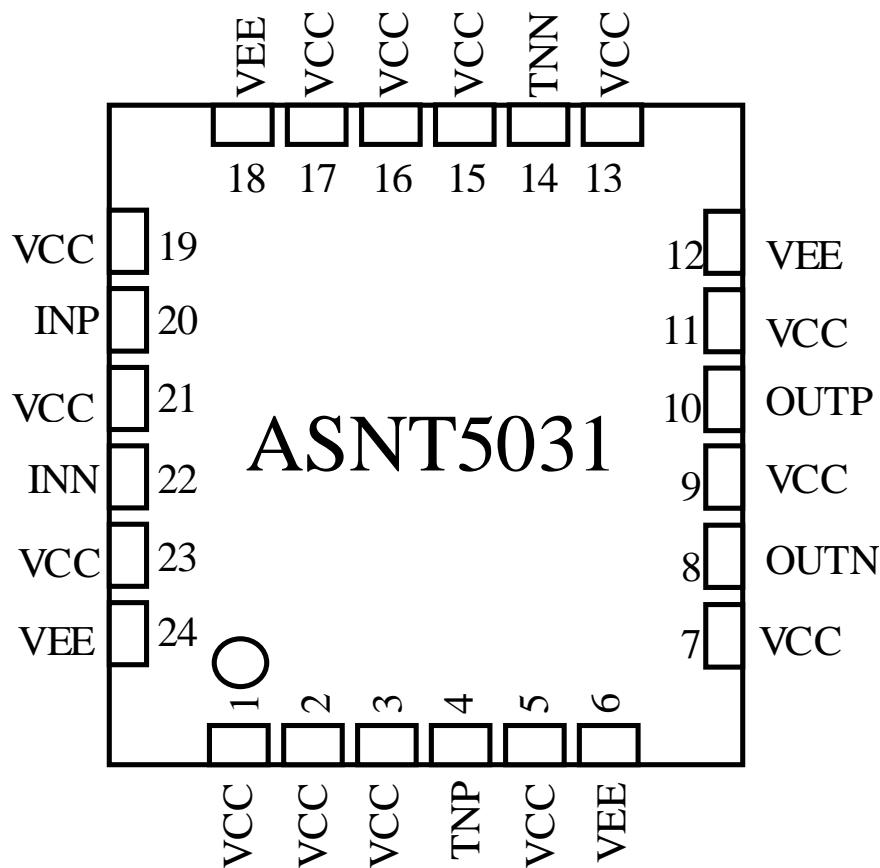




ASNT5031-PQC

17Gbps Limiting Amplifier / VCSEL Driver

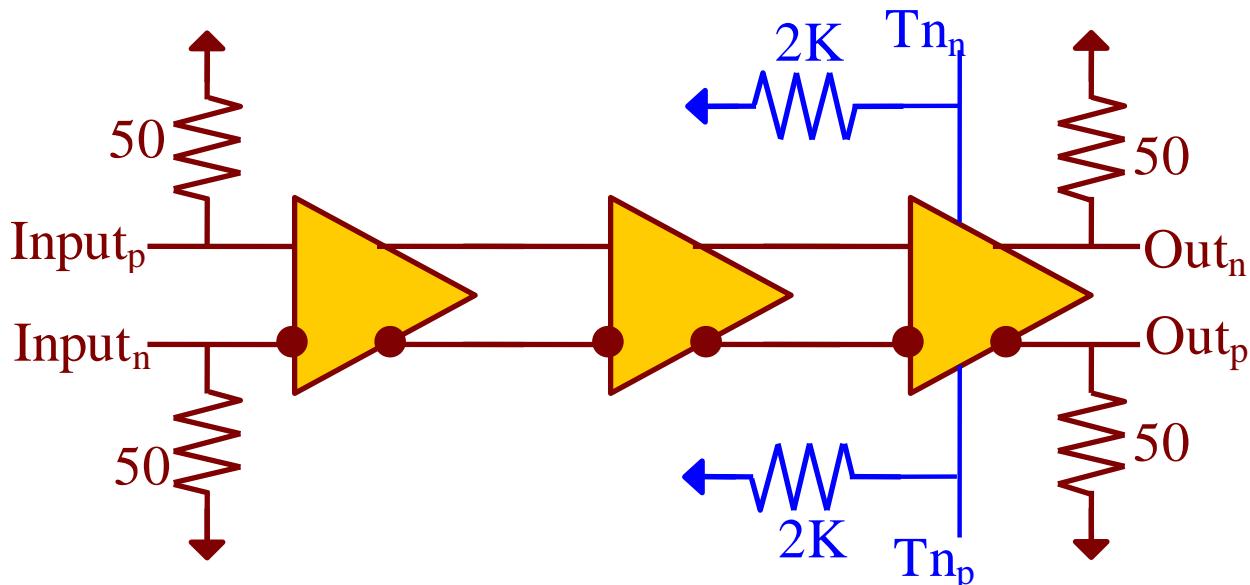
- Broadband (DC-17Gbps) limiting amplifier featuring output signal amplitude adjustment from 0.0V to 1.0V single ended.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 100MHz of bandwidth for the amplitude adjustment tuning port.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with nominal 500mV single-ended swing.
- Single ±5.0V power supply.
- Power consumption: 1.05W.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



DESCRIPTION

The temperature stable ASNT5031-PQC SiGe IC provides extremely low jitter broadband signal amplitude control capability between its input and output signal ports and is intended for use in high-speed measurement / test equipment. ASNT5031-PQC can process an up to 17Gbps data signal and deliver output signal amplitudes between 0.0V-1.0V through the up to 100MHz external adjustment of its differential tuning port. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±5.0V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

| TERMINAL | TYPE | DESCRIPTION |
|--|--------|---|
| NAME (NO.) | | |
| vcc 1,2,3,5,7,9,11 13,15,16,17,19,21,23 | PS | Power Supply: 5V / 0V |
| vee 6,12,18,24 | PS | Power Supply: 0V / -5V |
| inp 20 | Input | Differential CML high-speed data signal inputs |
| inn 22 | | |
| outp 10 | Output | Differential CML high-speed data signal outputs |
| outn 8 | | |
| tnp 4 | Input | Differential low-speed amplitude adjustment tuning inputs |
| tnn 14 | | |



ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|-------------------------|---------|------------|---------|------|--------------|
| VEE | -4.5 | 0.0 / -5.0 | -5.5 | V | $\pm 10\%$ |
| VCC | 4.5 | 5.0 / 0.0 | 5.5 | V | $\pm 10\%$ |
| IEE | | 210 | | mA | |
| Power | | 1.05 | | mW | |
| Junction Temp. | -25 | 50 | 125 | °C | |
| Input (in) | | | | | |
| Frequency | | 0.0 | 17 | Gbps | |
| CM Level | Vcc-0.8 | Vcc-0.2 | Vcc | V | |
| Swing (Diff or SE) | 50 | 400 | 1000 | mV | Peak-to-Peak |
| Output (out) | | | | | |
| Frequency | | 0.0 | 17 | Gbps | |
| CM Level* | Vcc-0.3 | Vcc-0.25 | Vcc-0.2 | V | |
| SE Swing* | 475 | 500 | 525 | mV | Peak-to-Peak |
| Rise/Fall Times* | 15 | 17 | 19 | ps | 20%-80% |
| Additive Jitter | | TBD | | ps | Peak-to-Peak |
| Tuning Port (tn) | | | | | |
| Diff. Swing | | -500 | 500 | mV | Peak-to-Peak |
| CM Level | Vcc-0.5 | Vcc-0.25 | Vcc | V | |
| Amplitude Variation | 0.0 | 500 | 1000 | mV | |
| CM Level | Vcc-0.5 | Vcc-0.25 | Vcc | V | |
| Bandwidth | 0.0 | | 100 | MHz | |

* Tuning pins are not connected (NC)

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's [website](#).