ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

Offices: 310-377-6029 / 310-803-9284 Fax: 310-377-9940
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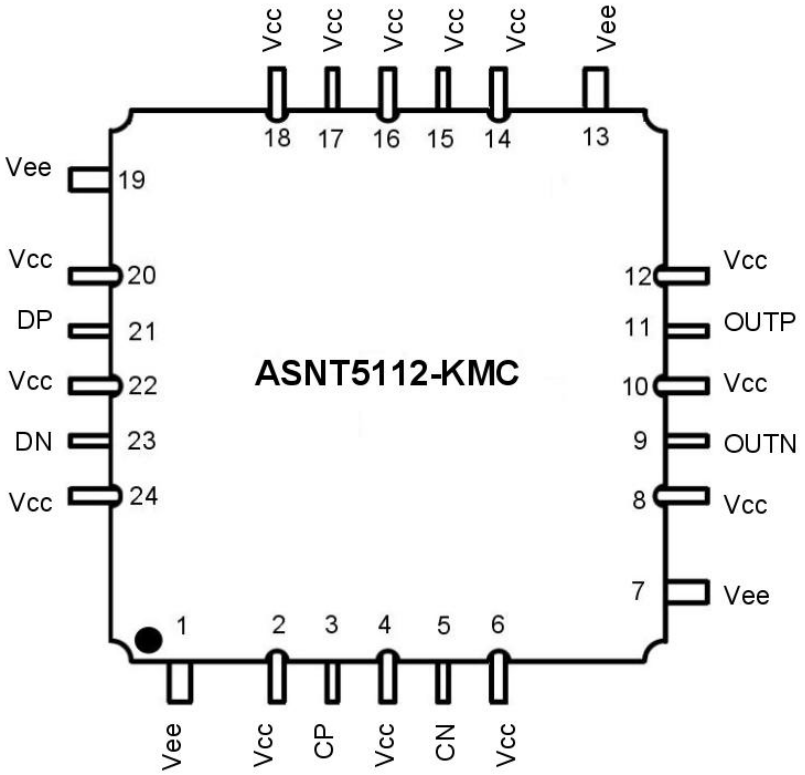
ASNT5112-KMC
High Sensitivity 32*Gbps* D-Type Flip-Flop

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock.
- Sensitive input data buffer with increased CM range that is ideal for sampling applications.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 32*GHz* analog input bandwidth for both clock and data.
- 4*ps* set-up/hold time capability.
- 88% clock phase margin for retiming of data input eye.
- Fully differential CML input interfaces.
- Fully differential CML output interface with 400*mV* single-ended swing.
- Single +3.3*V* or -3.3*V* power supply.
- Power consumption: 345*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.



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DESCRIPTION

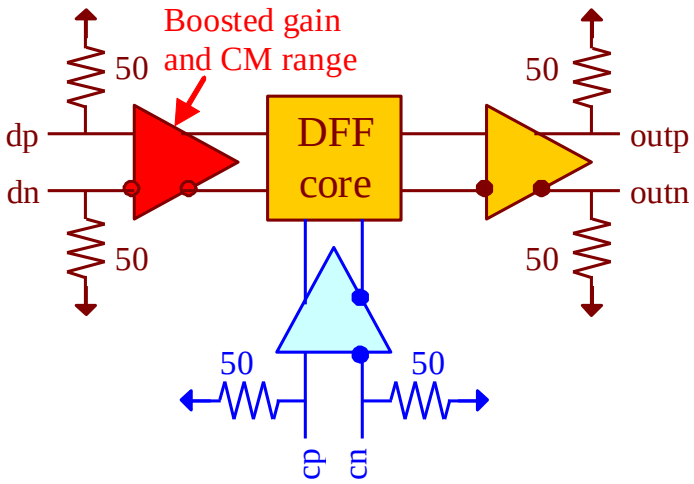

Fig. 1. Functional Block Diagram

The temperature stable ASNT5112-KMC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can sample an up to 32*Gbps* data signal ("dp/dn") with an up to 32*GHz* clock source ("cp/cn") to create a 32*Gbps* retimed NRZ data output ("outp/outn"). The data input buffer is designed to have increased input signal sensitivity and is able to operate over a wider range of input common mode (CM) voltages. The part's I/O's support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination.

POWER SUPPLY CONFIGURATION

The ASNT5112-KMC can operate with either a negative supply ("vcc" = 0.0*V*=ground and "vee" = -3.3*V*), or a positive supply ("vcc" = +3.3*V* and "vee" = 0.0*V*=ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume "vcc" = 0.0*V* and "vee" = -3.3*V*.

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed "vcc").

Table 1. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Supply Voltage ("vee")		-3.6	*V*
Power Consumption		0.4	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL		**TYPE**	**DESCRIPTION**
NAME	**(NO.)**		
vcc	2,4,6,8,10,12 14-18,20,22,24	PS	Positive power supply or ground
vee	1,7,13,19	PS	Ground or negative power supply
dp	21	Input	Differential CML high-speed data signals
dn	23		
cp	3	Input	Differential CML high-speed clock signals
cn	5		
outp	11	Output	Differential CML high-speed data signals
outn	9		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
Ivee		105		mA	
Power		345		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d) Frequency	0.0		32	Gbps	
CM Level	Vcc-1.5	Vcc-0.3	Vcc+0.3	V	
SE Swing	25	300	800	mV	Peak-to-peak
Input Clock (c) Frequency	0.0		32	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-peak
Duty Cycle	40%	50%	60%		
Output Data (out) Frequency	0.0		32	Gbps	
SE Swing	380	400	420	mV	Peak-to-peak
CM Level	"vcc"-(SE swing)/2			*V*	
Rise/Fall Times			13	ps	20%-80%
Additive Jitter			2.5	ps	Peak-to-peak
Clock Phase Margin	80%	85%	90%		

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package. The package's mechanical information is available on the company's website. Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the "vcc" plain, which is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT5112-KMC. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

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REVISION HISTORY

Revision	Date	Changes
3.1	2-2012	Revised Power Supply Configuration section Revised Package Information section
3.0	1-2012	Added Power Supply Configuration text Added Absolute Maximum Ratings table Revised Electrical Characteristics section Revised Package Information section
2.0	2-2009	Revised Electrical Characteristics section Revised Package Information section
1.0	1-2009	First release