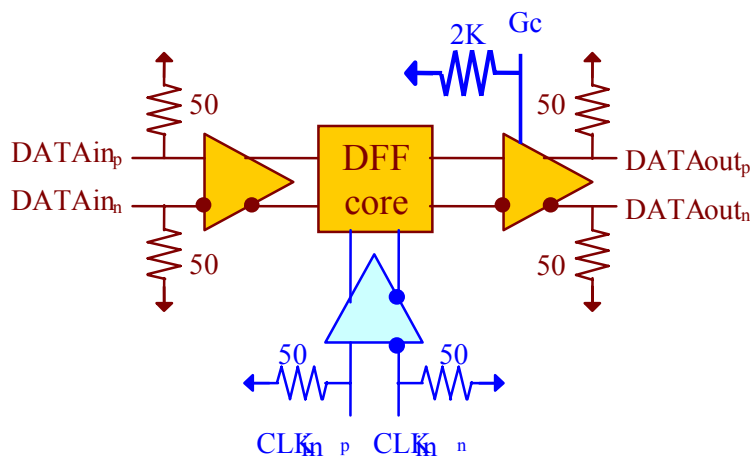


## ASNT5014-KMC

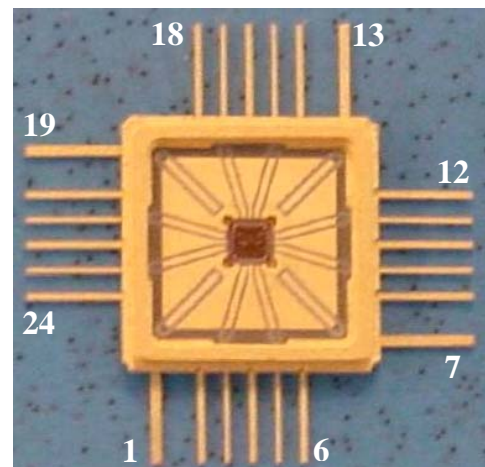
### 25Gbps D-Type Flip-Flop with Gain Control

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock and single-ended gain control.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 25GHz analog input bandwidth for both clock and data inputs.
- 6.5ps set-up/hold time capability.
- 87% clock phase margin for retiming of data input eye.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with variable gain control delivering 0.0V-1.0V single-ended.
- Single -3.3V power supply.
- Power consumption: 725mW.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

### DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT5014-KMC SiGe IC provides broadband data retiming with gain control functionality and is intended for use in high-speed measurement / test equipment. ASNT5014-KMC can sample an up to 25Gbps data signal with an up to 25GHz clock source to create a 25Gbps retimed NRZ data with output signal amplitudes between 0.0V-1.0V. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.



## TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	(NO.)		
vcc	2,4,6,8,10,12 14,16-18,20,22,24	PS	Power Supply: 0V (GND)
vee	1,7,13,19	PS	Power Supply: -3.3V
dp	21	Input	Differential CML high-speed data signal inputs
dn	23		
cp	3	Input	Differential CML high-speed clock signal inputs
cn	5		
outp	11	Output	Differential CML high-speed data signal outputs
outn	9		
gc	15	Input	Single-ended gain control input

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>VEE</b>	-3.1	-3.3	-3.5	V	±6%
<b>VCC</b>		0.0		V	
<b>IEE</b>		220		mA	
<b>Power</b>		725		mW	
<b>Junction Temp.</b>	-25	50	125	°C	
<b>Input Data (d)</b>					
Frequency	0.0		15	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
<b>Input Clock (c)</b>					
Frequency	0.0		15	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
<b>Output Data (out)</b>					
Frequency	0.0		15	Gbps	
CM Level	Vcc – (half the SE Swing)			V	
SE Swing	0		1000	mV	Peak-to-Peak
Rise/Fall Times			<18	ps	20%-80%
Jitter			<5	ps	Peak-to-Peak
Clock Phase Margin	80%	85%	90%		
<b>Tuning Port (gc)</b>					
Control voltage	-1		0	V	

## PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's [website](#).