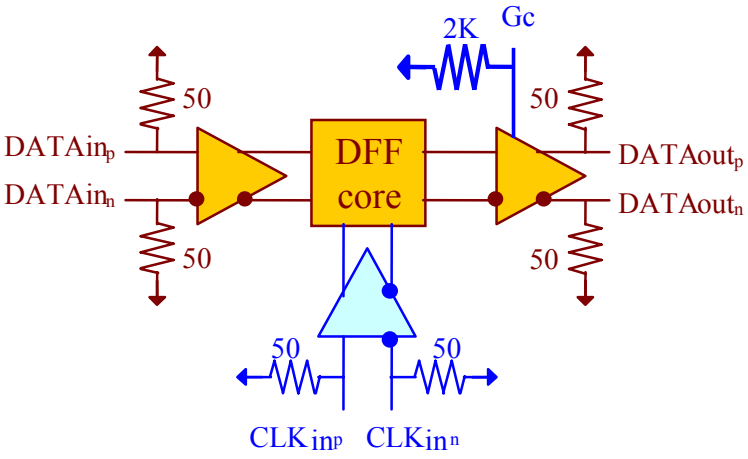
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

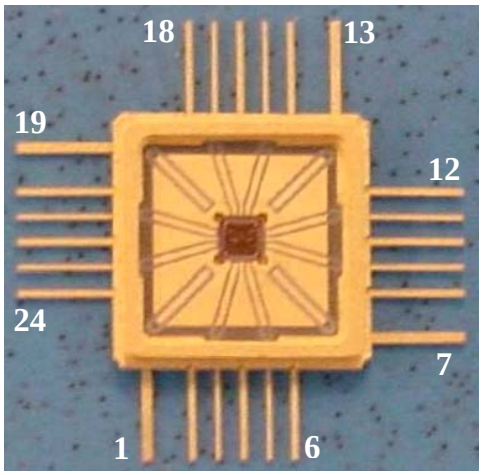
ASNT5013-KMC
30*Gbps* D-Type Flip-Flop with Gain Control

- High speed broadband D-Type Flip-Flip for data retiming with full rate clock and single-ended gain control.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 30*GHz* analog input bandwidth for both clock and data inputs.
- 6.5*ps* set-up/hold time capability.
- 87% clock phase margin for retiming of data input eye.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with variable gain control delivering 0.0*V*-0.7*V* single-ended.
- Single -3.3*V* power supply.
- Power consumption: 510*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT5013-KMC SiGe IC provides broadband data retiming with gain control functionality and is intended for use in high-speed measurement / test equipment. ASNT5013-KMC can sample an up to 30*Gbps* data signal with an up to 30*GHz* clock source to create a 30*Gbps* retimed NRZ data with output signal amplitudes between 0.0V-0.7V. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.

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TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	2,4,6,8,10,12 14,16-18,20,22,24	PS	Power Supply: 0V (GND)
vee	1,7,13,19	PS	Power Supply: -3.3V
dp	21	Input	Differential CML high-speed data signal inputs
dn	23		
cp	3	Input	Differential CML high-speed clock signal inputs
cn	5		
outp	11	Output	Differential CML high-speed data signal outputs
outn	9		
gc	15	Input	Single-ended gain control input

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		155		mA	
Power		510		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d) Frequency	0.0		20	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Input Clock (c) Frequency	0.0		20	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
Output Data (out) Frequency	0.0		20	Gbps	
CM Level	Vcc – (half the SE Swing)			V	
SE Swing	0		700	mV	Peak-to-Peak
Rise/Fall Times			<15	ps	20%-80%
Jitter			<5	ps	Peak-to-Peak
Clock Phase Margin	80%	85%	90%		
Tuning Port (gc) Control voltage	-1		0	V	

PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's website.