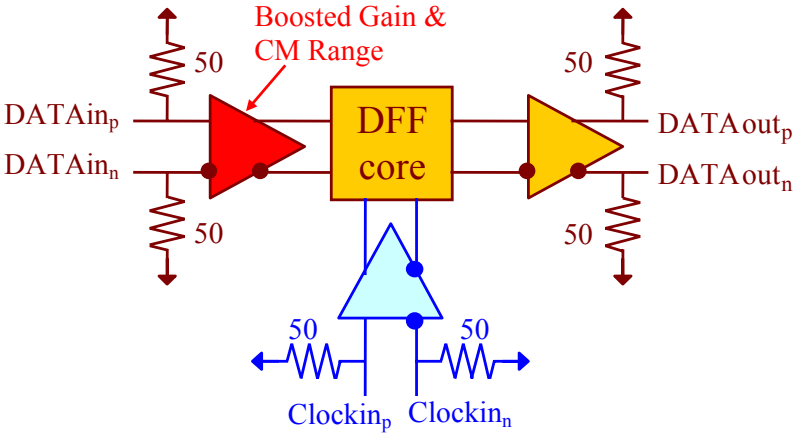
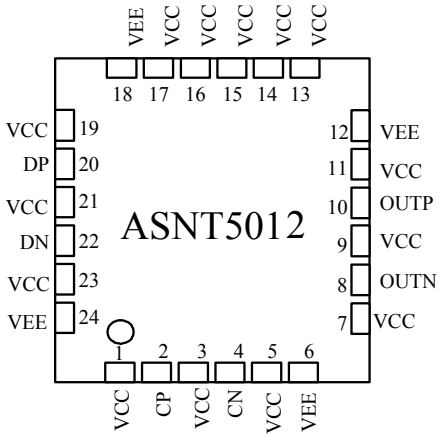
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5012-PQC
14*Gbps* D-Type Flip-Flop with Increased Input Signal Sensitivity

- High speed broadband D-Type Flip-Flop for data retiming with full rate clock.
- Sensitive input data buffer with increased CM range that is ideal for sampling applications.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 14*GHz* analog input bandwidth for both clock and data.
- 8*ps* set-up/hold time capability.
- 89% clock phase margin for retiming of data input eye.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single -3.3*V* power supply.
- Power consumption: 465*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



Functional Block Diagram



Package Pins

DESCRIPTION

The temperature stable ASNT5012-PQC SiGe IC provides broadband data retiming functionality and is intended for use in high-speed measurement / test equipment. ASNT5012-PQC can sample an up to 14*Gbps* data signal with an up to 14*GHz* clock source to create a 14*Gbps* retimed NRZ data output. The data input buffer is designed to have increased input signal sensitivity and is able to operate over a wider range of input common mode (CM) voltages. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.

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TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	(NO.)		
vcc	1,3,5,7,9,11 13-17,19,21,23	PS	Power Supply: 0V (GND)
vee	6,12,18,24	PS	Power Supply: -3.3V
dp	20	Input	Differential CML high-speed data signal inputs
dn	22		
cp	2	Input	Differential CML high-speed clock signal inputs
cn	4		
outp	10	Output	Differential CML high-speed data signal outputs
outn	8		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		140		mA	
Power		465		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d) Frequency	0.0		14	Gbps	
CM Level	Vcc-1.5	Vcc-0.3	Vcc+0.3	V	
SE Swing	25	300	800	mV	Peak-to-Peak
Input Clock (c) Frequency	0.0		14	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
Output Data (out) Frequency	0.0		14	Gbps	
CM Level	Vcc-0.3	Vcc-0.2	Vcc-0.1	V	
SE Swing	380	400	420	mV	Peak-to-Peak
Rise/Fall Times			<22	ps	20%-80%
Additive Jitter			<10	ps	Peak-to-Peak
Clock Phase Margin	80%	85%	90%		

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.