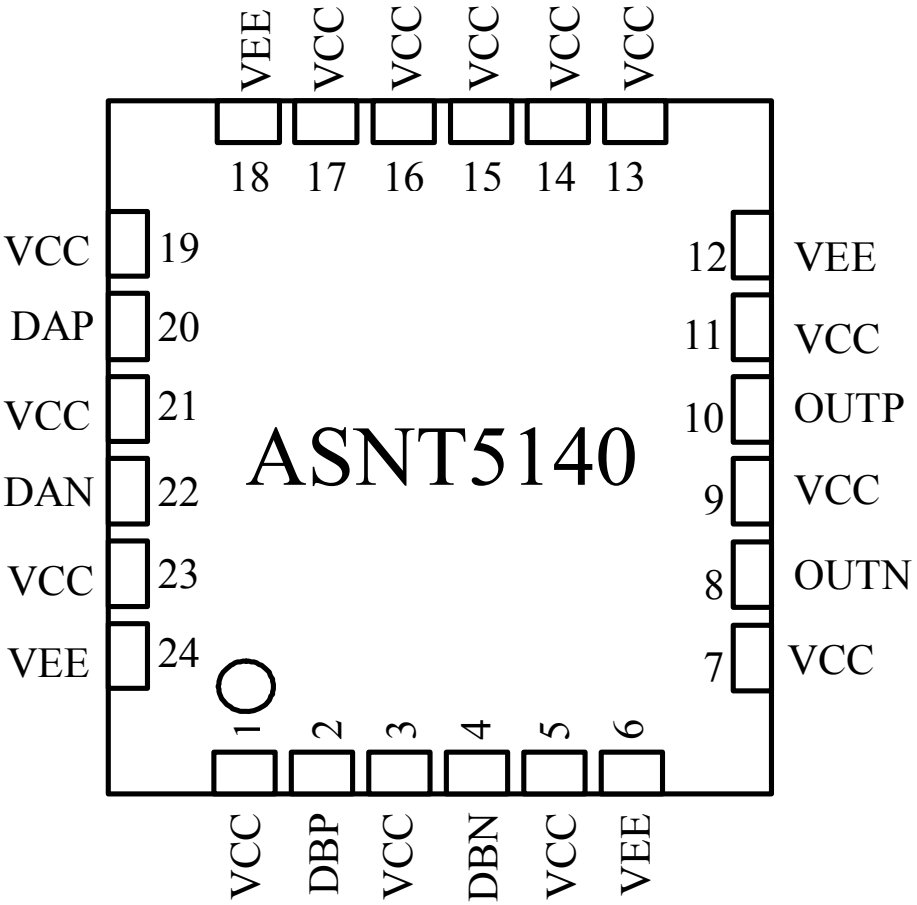
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5140-PQC
14*GHz* XOR Logic Gate

- High speed broadband Exclusive-OR (XOR) Boolean logic gate.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 14*GHz* analog input bandwidth for both data inputs.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 270*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



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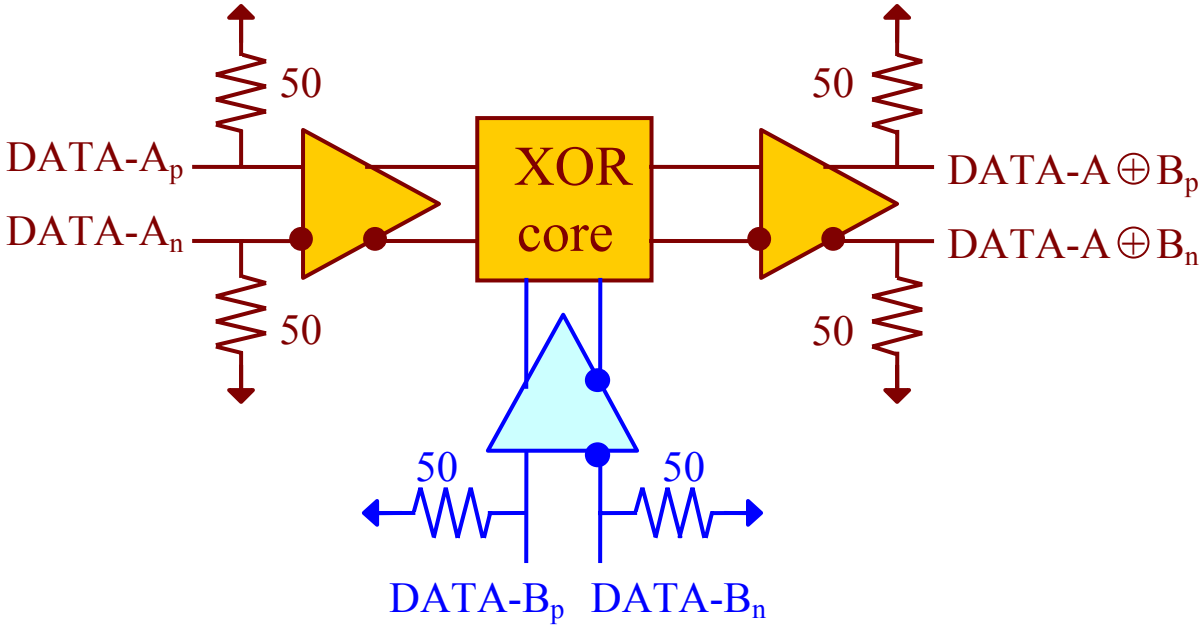
DESCRIPTION

The temperature stable ASNT5140-PQC SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality and is intended for use in high-speed measurement / test equipment. ASNT5140-PQC can XOR an up to 7*GHz* clock signal with another up to 7*GHz* clock signal to create an up to 14*GHz* clock output signal. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11 13-17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
dap	20	Input	Differential CML high-speed signal inputs
dan	22		
dbp	2	Input	Differential CML high-speed signal inputs
dbn	4		
outp	10	Output	Differential CML high-speed signal outputs
outn	8		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		82		mA	
Power		270		mW	
Junction Temp.	-25	50	125	°C	
Inputs (d)					
Frequency	0.0		14	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-peak
Output (out)					
Frequency	0.0		14	GHz	
CM Level	Vcc-0.3	Vcc-0.2	Vcc-0.1	V	
SE Swing	380	400	420	mV	Peak-to-peak
Rise/Fall Times	15	17	19	ps	20%-80%
Additive Jitter			<1	ps	Peak-to-peak

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.