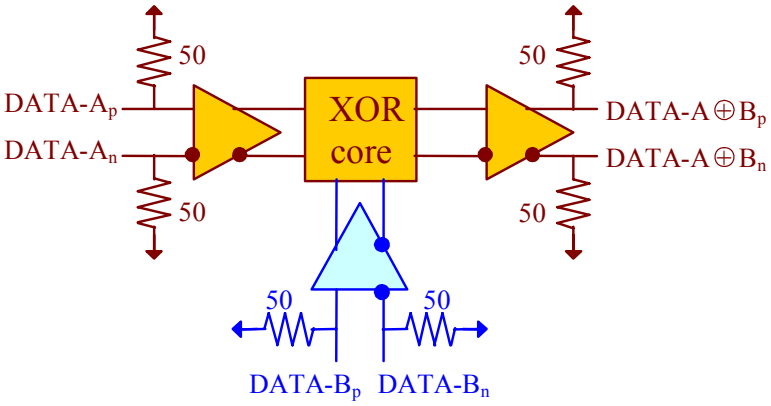
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

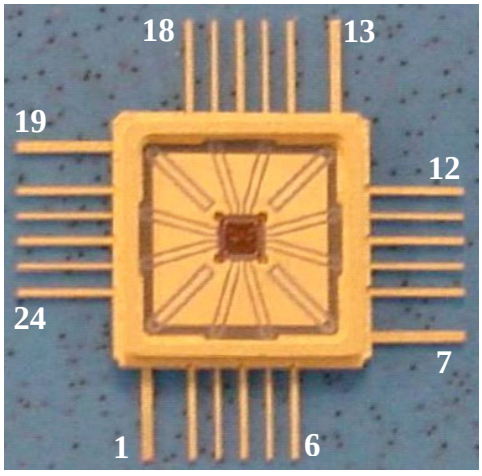
ASNT5040-KMC
25*GHz* XOR Logic Gate

- High speed broadband Exclusive-OR (XOR) Boolean logic gate.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 25*GHz* analog input bandwidth for both data inputs.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single -3.3*V* power supply.
- Power consumption: 415*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT5040-KMC SiGe IC provides broadband Exclusive-OR (XOR) Boolean logic functionality and is intended for use in high-speed measurement / test equipment. ASNT5040-KMC can XOR an up to 12.5*GHz* clock signal with another up to 12.5*GHz* clock signal to create an up to 25*GHz* clock output signal. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.

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TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	2,4,6,8,10,12 14-18,20,22,24	PS	Power Supply: 0V
vee	1,7,13,19	PS	Power Supply: -3.3V
dap	21	Input	Differential CML high-speed signal inputs
dan	23		
dbp	3	Input	Differential CML high-speed signal inputs
dbn	5		
outp	11	Output	Differential CML high-speed signal outputs
outn	9		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		125		mA	
Power		415		mW	
Junction Temp.	-25	50	125	°C	
Inputs (d)					
Frequency	0.0		25	GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
SE Swing	50	400	1000	mV	Peak-to-Peak
Output (out)					
Frequency	0.0		25	GHz	
CM Level	Vcc-0.25	Vcc-0.2	Vcc-0.15	V	
SE Swing	380	400	420	mV	Peak-to-Peak
Rise/Fall Times	6	8	10	ps	20%-80%
Additive Jitter		TBD		ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal

PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's website.