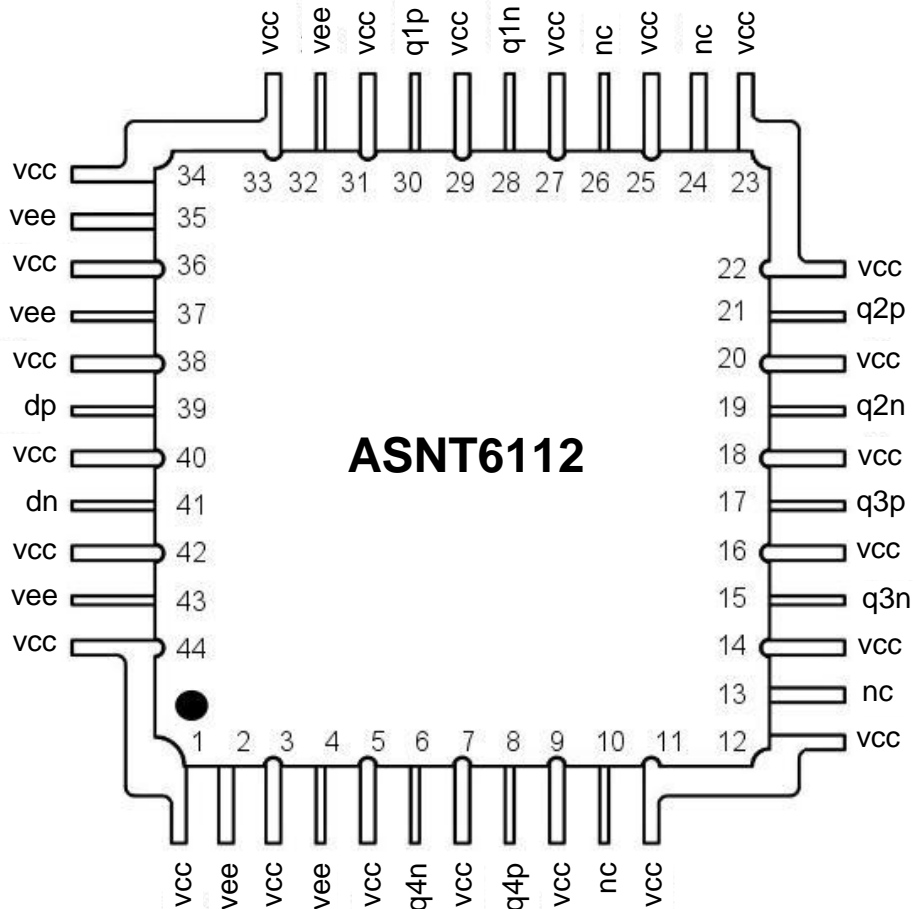




## ASNT6112-KMM DC-25GHz 1-to-4 Analog Signal Splitter

- DC to 25GHz broadband linear signal splitter
- One differential CML-type input port and four phase-matched differential CML-type output ports
- Differential input linearity range up to 500mV p-p
- Differential gain of approximately -1.5dB
- Low jitter and limited temperature variation over industrial temperature range
- Single +3.3V or -3.3V power supply
- Power consumption: 1.35W
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 44-pin package





## DESCRIPTION

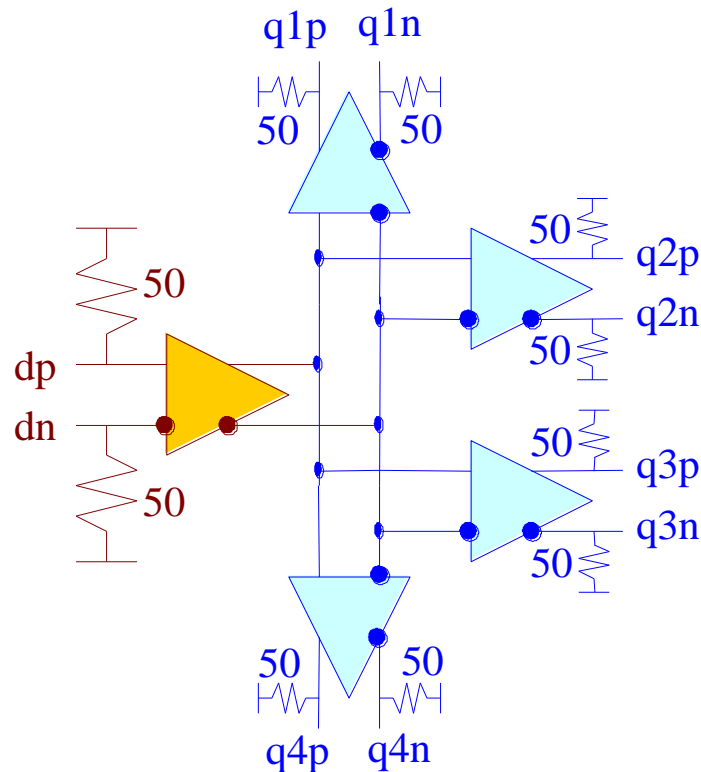


Fig. 1. Functional Block Diagram

The temperature stable ASNT6112-KMM 1-to-4 analog signal splitter is intended for use in high-speed interleaved ADCs or similar systems. The IC shown in Fig. 1 can receive a broad-band analog signal at its differential input *dp/dn* and effectively distribute it to four separate phase-matched differential outputs *q1p/q1n*, *q2p/q2n*, *q3p/q3n*, *q4p/q4n* with a nominal gain of 0dB.

The part's I/O's support the CML logic interface with on chip 50 $\Omega$  termination to *vcc* and may be used differentially, AC/DC coupled, single-ended, or in any combination (also see POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance. In particular, the specified output common-mode voltage level is guaranteed only in case of external single-ended 50 $\Omega$  DC termination to *vcc*.

## POWER SUPPLY CONFIGURATION

The part can operate with either negative supply (*vcc* = 0.0V = ground and *vee* = -3.3V), or positive supply (*vcc* = +3.3V and *vee* = 0.0V = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with 50 $\Omega$  termination to ground. In any case, the input common mode voltage level is shifted down from *vcc* by a certain voltage of  $\Delta V_{ICM}$  as specified in ELECTRICAL CHARACTERISTICS. To have the input common mode voltage equal to ground, a floating negative supply scheme detailed in Fig. 2 should be used.

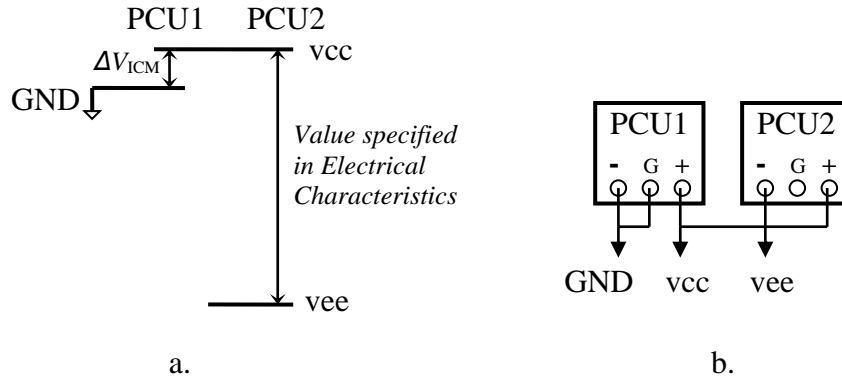


Fig. 2. Floating Negative Supply Scheme: Potential Diagram (a) and Schematic (b)

For the best performance, the external 50Ω terminations for the outputs should be connected to vcc, but not to ground!

Different PCB layouts will be needed for each different power supply combination.

**All the characteristics detailed below assume vcc = 0.0V and vee = -3.3V.**

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	V
Power Consumption		1.49	W
RF Input Voltage Swing (SE)		1.4	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%



## TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
<b>High-Speed I/Os</b>			
dp	39	CML input	Differential high speed data inputs with internal SE 50Ohm termination to vcc
dn	41		
q1p	30	CML output	Differential high speed data outputs with internal SE 50Ohm termination to vcc. Require external SE 50Ohm termination to vcc
q1n	28		
q2p	21		
q2n	19		
q3p	17		
q3n	15		
q4p	8		
q4n	6		
<b>Supply and Termination Voltages</b>			
Name	Description		Pin Number
vcc	Positive power supply (+3.3V or 0)		1, 3, 5, 7, 9, 11, 12, 14, 16, 18, 20, 22, 23, 25, 27, 29, 31, 33, 34, 36, 38, 40, 42, 44
vee	Negative power supply (0V or -3.3V)		2, 4, 32, 35, 37, 43
n/c	Not connected pins		10, 13, 24, 26

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-3.1	-3.3	-3.5	V	±6%
vcc		0.0		V	External ground
I <sub>vee</sub>		410		mA	
Power consumption		1350		mW	
Junction temperature	-25	50	125	°C	
<b>Input Analog (dp/dn)</b>					
Bandwidth	DC		25	GHz	-3dB
Common mode level	vcc-0.6	vcc-0.5	vcc-0.4	mV	
Input Noise Density		1.5		nV/sqrt(Hz)	
S <sub>11</sub>		-10		dB	DC to 30GHz
<b>Output Analog (q1p/q1n, q2p/q2n, q3p/q3n, q4p/q4n)</b>					
Common mode level		vcc-0.55		V	With external 50Ohm DC termination
S <sub>22</sub>		-8		dB	DC to 30GHz
Small Signal Differential Gain	-2		-1	dB	at 10GHz
Output referred 1dB Compression Point		2.7		dBm	Single-Ended, 20GHz
THD		-45		dBc	at 10GHz



## PACKAGE INFORMATION

The chip die is housed in a custom 44-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6112-KMM. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

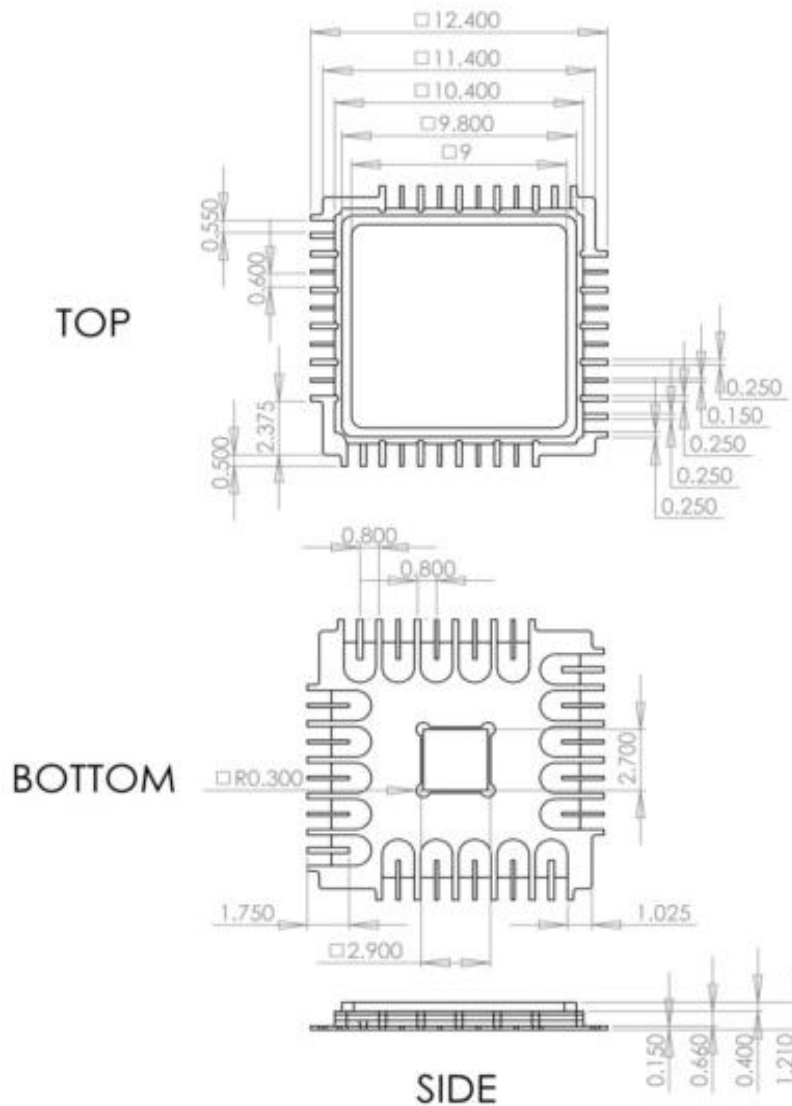


Fig. 3. CQFP 44-Pin Package Drawing (All Dimensions in mm)



This device complies with Commission Delegated Directive (EU) 2015/863 of 4 June 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council as regards the list of restricted substances (Text with EEA relevance) on the restriction of the use of certain hazardous substances in electrical and electronics equipment (RoHS Directive) in accordance with the definitions set forth in the directives for all ten substances.

## REVISION HISTORY

Revision	Date	Changes
2.5.2	11-2020	Corrected linearity range
2.4.2	05-2020	Updated Package Information
2.3.2	07-2019	Updated Letterhead
2.3.1	05-2015	Revised Package Information section Updated format
2.2.1	08-2014	Corrected Power Supply Configuration section Corrected gain values Corrected THD value
2.1.1	03-2013	Corrected functional block diagram Corrected description Corrected absolute maximum ratings table Corrected terminal functions table Corrected electrical characteristics table Updated package information
2.0	03-2012	Updated block diagram Revised description Updated electrical characteristics table
1.3	01-2012	Added mechanical drawing and packaging information
1.2	11-2011	Corrected terminal functions table
1.0	07-2011	Initial release