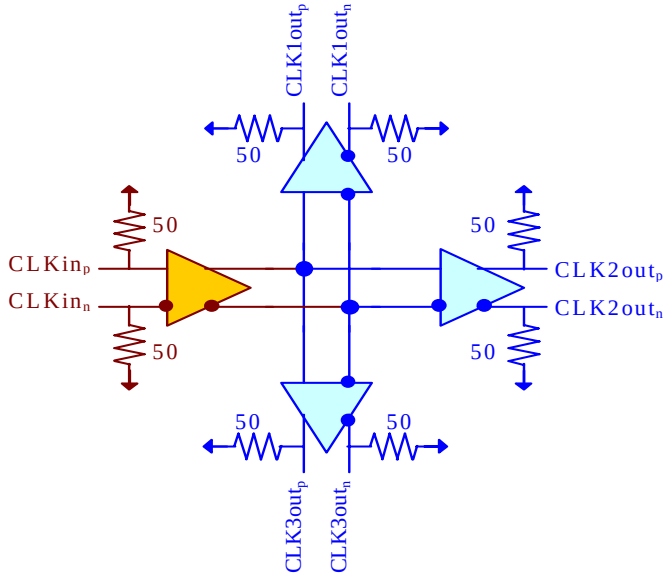
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

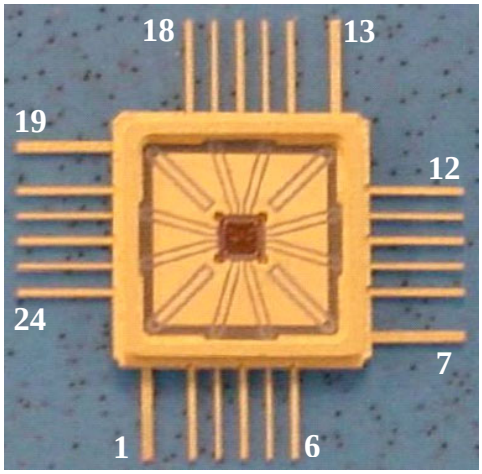
ASNT5121/5120-KMC
50*Gbps*-30*GHz* Data/Clock Distributor

- High-speed broadband Data/Clock Amplifier and Splitter for signal distribution.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 30*GHz* analog input bandwidth.
- One input signal port and three amplified output signal ports.
- On-chip matched phase delays for all outputs.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single -3.3*V* power supply.
- Power consumption: 580*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 24-pin package.

DESCRIPTION



Functional Block Diagram



Package View

The temperature stable ASNT5121-PQC SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. ASNT5121-PQC can receive an up to 50*Gbps*-30*GHz* data/clock signal and effectively distribute it to three separate phase matched outputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3*V* power supply.

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TERMINAL FUNCTIONS

vcc vee	2,4,6,8,10,12 14,16,18,20,22,24 1,7,13,19	PS PS	Power Supply: 0V Power Supply: -3.3V
clkip clkin	21 23	Input	Differential CML high-speed signal inputs
clko1p clko1n	17 15	Output	Differential CML high-speed signal outputs
clko2p clko2n	11 9	Output	Differential CML high-speed signal outputs
clko3p	3	Output	Differential CML high-speed signal outputs

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	±6%
IEE		175		mA	
Power		580		mW	
Junction Temp.	-25	50	125	°C	
Input Data-Clock (clki)					
Data rate/Frequency	0.0		50/30	Gbps-GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
Swing (Diff or SE)	50	400	1000	mV	Peak-to-peak
Duty Cycle	40%	50%	60%		For clock signal
Out Data-Clock (clko)					
Data rate/Frequency	0.0		50/30	Gbps-GHz	
CM Level	Vcc-0.35	Vcc-0.3	Vcc-0.25	V	
SE Swing	380	400	420	mV	Peak-to-peak
Rise/Fall Times	6	8	10	ps	20%-80%
Additive Jitter			<1	ps	Peak-to-peak
Duty Cycle	45%	50%	55%		For clock signal

PACKAGE INFORMATION

The chip is packaged in ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package's mechanical information is available on the company's website.