ADSANTEC
Ultra High-Speed Mixed Signal ASICs
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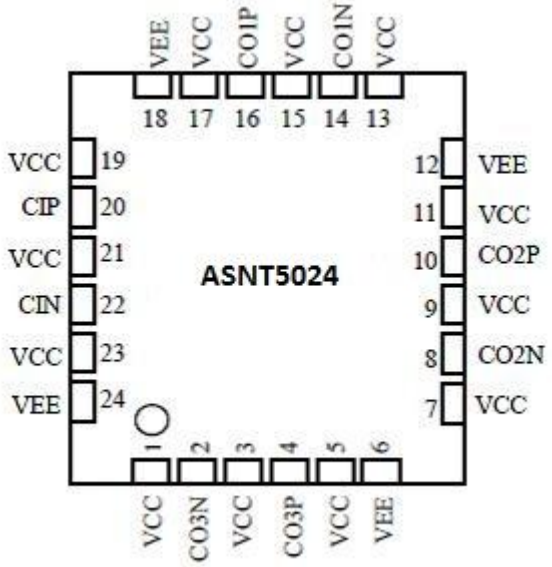
ASNT5024-PQC
17Gb/s-17GHz 1:3 Data/Clock Distributor.

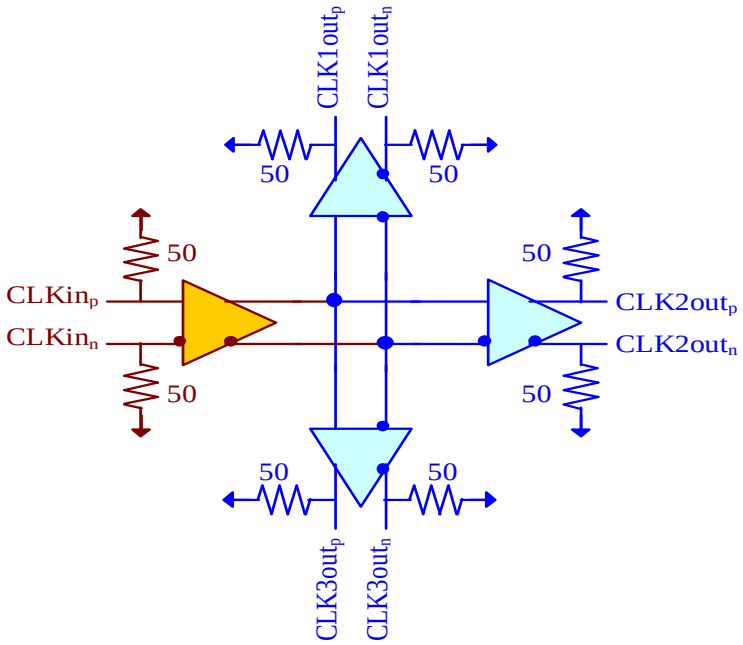
- High-speed broadband Data/Clock Amplifier and Splitter for signal distribution.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 17GHz analog input bandwidth
- One input signal port and three amplified output signal ports.
- On-chip matched phase delays for all outputs.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 600*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 780*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



DESCRIPTION

The temperature stable ASNT5024-PQC SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. ASNT5024-PQC can receive an up to 17*Gbps*-17*GHz* data/clock signal and effectively distribute it to three separate phase matched outputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3*V* power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11 13,15,17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
cip	20	Input	Differential CML high-speed signal inputs
cin	22		
co1p	16	Output	Differential CML high-speed signal outputs
co1n	14		
co2p	10	Output	Differential CML high-speed signal outputs
co2n	8		
co3p	4	Output	Differential CML high-speed signal outputs
co3n	2		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		235		mA	
Power		780		mW	
Junction Temp.	-25	50	125	°C	
Input Data-Clock (ci)					
Data rate/Frequency	0.0		17/17	Gbps-GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
Swing (Diff or SE)	50	400	1000	mV	Peak-to-peak
Duty Cycle	40%	50%	60%		For clock signal
Out Data-Clock (co)					
Data rate/Frequency	0.0		17/17	Gbps-GHz	
CM Level	Vcc-0.35	Vcc-0.3	Vcc-0.25	V	
SE Swing	570	600	630	mV	Peak-to-peak
Rise/Fall Times	15	17	19	ps	20%-80%
Additive Jitter			5	ps	Peak-to-peak
Duty Cycle	45%	50%	55%		For clock signal

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package The package's mechanical information is available on the company's website.

REVISION HISTORY

Revision	Date	Changes
Rev 1.3	1-2012	Modified Electrical characteristics table Modified Title and description
Rev 1.2	12-2011	Modified Electrical characteristics table Modified Title and description Added Revision history table
Rev 1.1	8-2011	Initial Release