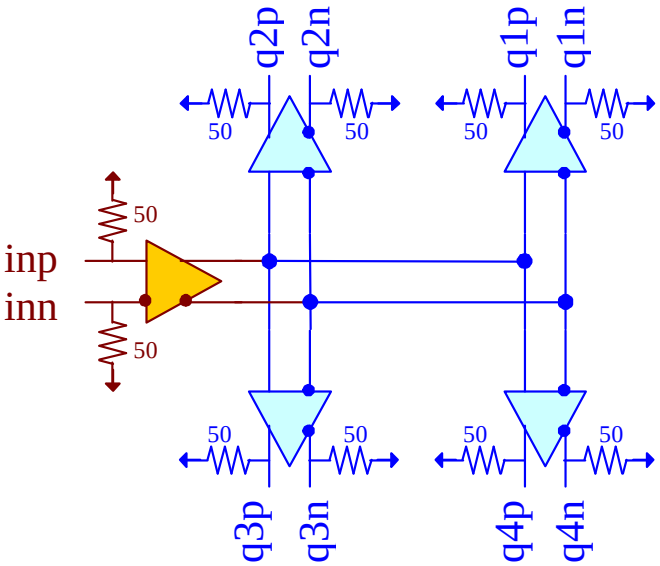
ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Sience And Novel Technologies Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275
Phone: 310-377-6029 / 310-803-9284 | Fax: 310-377-9940
Website: www.adsantec.com

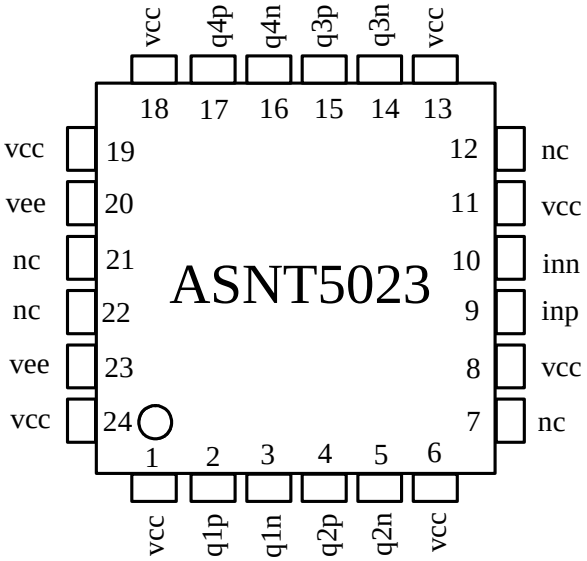
ASNT5023-PQC
17*Gbps*-14*GHz* Data/Clock Distributor

- High-speed broadband Data/Clock Amplifier and Splitter for signal distribution.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 14*GHz* analog input bandwidth.
- One input signal port and four amplified output signal ports.
- On-chip matched phase delays for all outputs.
- Fully differential input and output buffers with on-chip 50*Ohm* termination.
- Linearized data output for minimized undershoot/overshoot.
- CML output interface with 600*mV* single-ended swing.
- Single +3.3*V* or -3.3*V* power supply.
- Power consumption: 1060*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- MLF/QFN 24-pin package.

DESCRIPTION



Functional Block Diagram



Package Diagram

The temperature stable ASNT5023-PQC SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. ASNT5023-PQC can receive an up to 17*Gbps*-14*GHz* data/clock signal and effectively distribute it to four separate phase matched outputs. The part's I/Os support the CML logic interface with on chip 50*Ohm* termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single +3.3*V* or -3.3*V* power supply.

TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,6,8,11,13, 18,19,24	PS	Power Supply: 3.3V / 0V
vee	20,23	PS	Power Supply: 0V / -3.3V
inp	9	Input	Differential CML high-speed signal inputs
inn	10		
q1p	2	Output	Differential CML high-speed signal outputs
q1n	3		
q2p	4	Output	Differential CML high-speed signal outputs
q2n	5		
q3p	15	Output	Differential CML high-speed signal outputs
q3n	14		
q4p	17	Output	Differential CML high-speed signal outputs
q4n	16		

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Vee	-3.1	-3.3	-3.5	*V*	If Vcc = 0 (GND)
Vcc	3.1	3.3	3.5	*V*	If Vee = 0 (GND)
Ivee		320		*mA*	
Power		1060		*mW*	
Junction Temp.	-25	50	125	*°C*	
Input Data-Clock (in)					
Data rate/Clock frequency	0.0		17/14	*Gbps/GHz*	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	*V*	
Swing (Diff or SE)	50	400	1000	*mV*	Peak-to-Peak
Duty Cycle	40%	50%	60%		For clock signal
Out Data-Clock (qX)					
Data rate/Clock frequency	0.0		17/14	*Gbps/GHz*	
CM Level	Vcc-0.35	Vcc-0.3	Vcc-0.25	*V*	
SE Swing	570	600	630	*mV*	Peak-to-Peak
Rise/Fall Times	15	17	19	*ps*	20%-80%
Additive Jitter			5	*ps*	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.