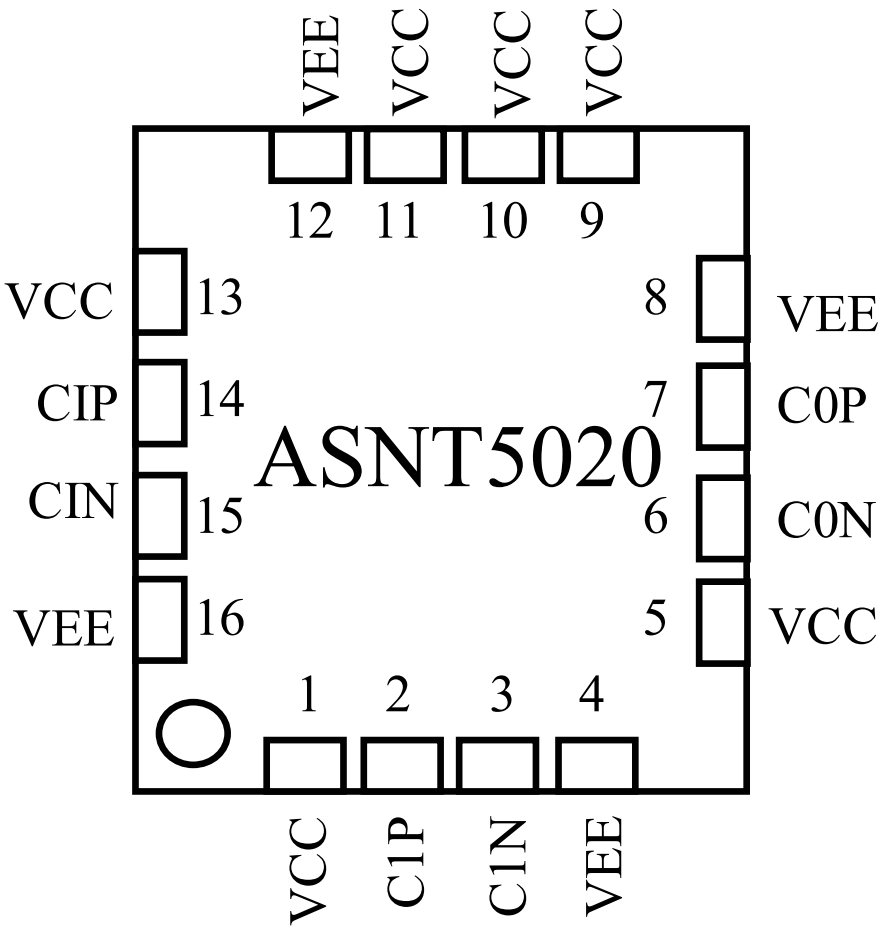
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5020-PQD
17*Gbps*-15*GHz* Data/Clock Distributor

- High-speed broadband Data/Clock Amplifier and Splitter for signal distribution.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- 15*GHz* analog input bandwidth.
- One input signal port and two amplified output signal ports.
- On-chip matched phase delays for both outputs.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 600*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 560*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 16-pin package.



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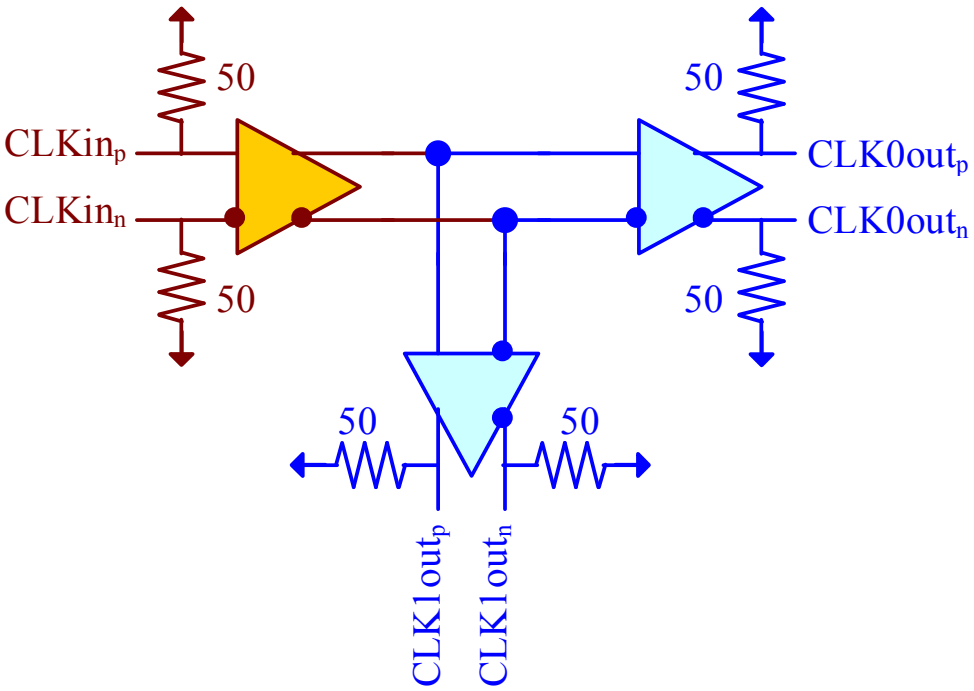
DESCRIPTION

The temperature stable ASNT5020-PQD SiGe IC provides active broadband data/clock signal splitting and is intended for use in high-speed measurement / test equipment. ASNT5020-PQD can receive an up to 17*Gbps*-15*GHz* data/clock signal and effectively distribute it to two separate phase matched outputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3*V* power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL (NO.)	TYPE	DESCRIPTION
vcc	1,5,9-11,13	PS	Power Supply: 3.3V / 0V
vee	4,8,12,16	PS	Power Supply: 0V / -3.3V
clkip	14	Input	Differential CML high-speed clock signal inputs
clkin	15		
clko0p	7	Output	Differential CML high-speed clock signal outputs
clko0n	6		
clko1p	2	Output	Differential CML high-speed clock signal outputs
clko1n	3		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	±6%
IEE		170		mA	
Power		560		mW	
Junction Temp.	-25	50	125	°C	
Input Data-Clock (ci)					
Data rate/clock frequency	0.0		17/15	Gbps/GHz	
CM Level	Vcc-0.8	Vcc-0.2	Vcc	V	
Swing (Diff or SE)	50	400	1000	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
Out Data-Clock (co)					
Data rate/Clock frequency	0.0		17/15	Gbps/GHz	
CM Level	Vcc-0.35	Vcc-0.3	Vcc-0.25	V	
SE Swing	570	600	630	mV	Peak-to-Peak
Rise/Fall Times	13	15	17	ps	20%-80%
Additive Jitter			5	ps	Peak-to-Peak
Duty Cycle	45%	50%	55%		For clock signal

PACKAGE INFORMATION

The chip is packaged in a standard 16-pin QFN package. The package's mechanical information is available on the company's website.