ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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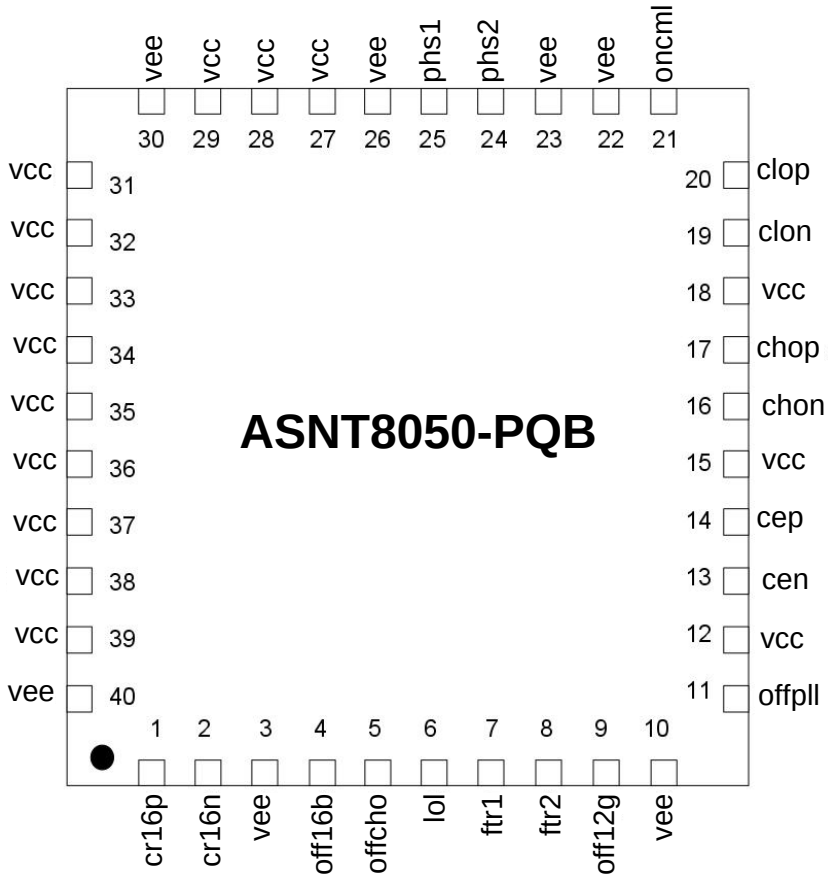
ASNT8050-PQB
Programmable PLL with Integrated 7.4-8.8*GHz* and 10.8-12.7*GHz* VCOs.

- Phase-Locked Loop with two selectable frequency ranges.
- Closed-Loop SSB PN at 10*MHz* offset better than 98*dB/Hz*.
- Selectable PLL divider ratio of 8 or 16.
- On-chip Loss-of-Lock control circuit.
- External RC loop filter.
- LVDS or CML input reference clock interface.
- Full-rate clock output.
- Clock-divided-by-16 LVDS output with 90°-step phase selection.
- Optional operational mode as a divider by 8 or by 16 with PLL disabled.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 670*mW* .
- Standard 40-pin QFN package with a thermal pad.



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DESCRIPTION

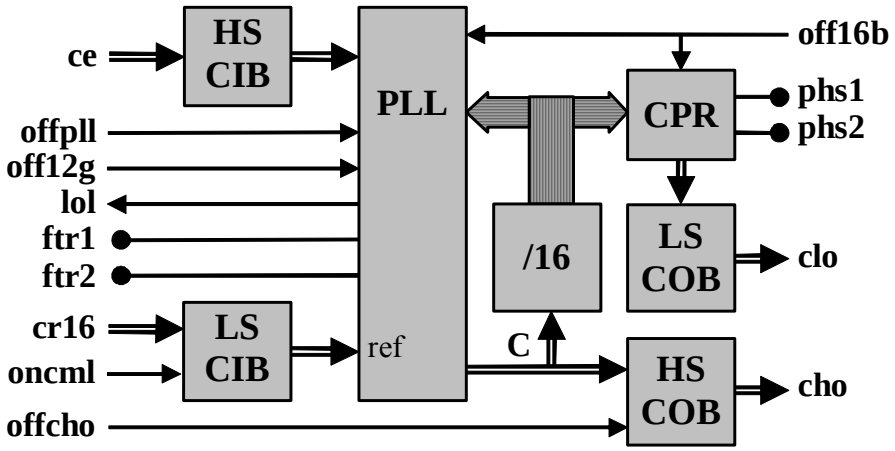

Fig. 1. Functional Block Diagram.

ASNT8050-PQB is a high-speed dual-range phase-locked loop (PLL) with additional control functions shown in Table 1. All functions are further described in the following sections.

Table 1. PLL Control Functions.

Control signal	Logic State			Described in.
	"0"	Not connected (default)	"1"	
"off12g"	Higher VCO range	Same as "0" state	Lower VCO range	PLL
"offcho"	HS COB enabled	Same as "0" state	HS COB disabled	HS COB
"phs1"/"phs2"	See Table 4			CPR
"off16b"	Clock division ratio of 16	Same as "0" state	Clock division ratio of 8	PLL, CPR
"offpll"	PLL enabled	Same as "0" state	PLL disabled	PLL
"oncml"	LVDS input interface	Same as "0" state	CML input interface	LS CIB

One of two PLL's frequency ranges can be selected by control signal "off12g". In the main operational mode, the IC shown in Fig. 1 accepts a low-speed reference clock ("cr16") with the frequency *f*/16 and converts it into high-speed output clock ("cho") with the frequency *f* and low-speed output clock ("clo") with the frequency *f*/16. The high-speed clock output buffer can be enabled/disabled by control signal "offcho". One of four 90° shifted phases of the low-speed output clock can be selected by control signals "phs1" and "phs2". Output control signal "lol" indicates the locked or unlocked state of the PLL.

The PLL can operate with the *f*/8 reference and output clocks as defined by control signal "off16b". In this mode, the phase selection of the output low-speed clock is not available. When operating in the closed-loop mode, the PLL requires external loop filter connected to pins "ftr1" and "ftr2". It can also operate in the open-loop mode with its voltage-controlled oscillator (VCO) controlled externally by voltages applied to the same pins. The chip can also operate as a divider of input high-speed clock "chi" if the PLL is disabled by control signal "offpll". The division ratio of 8 or 16 can be selected by control signal "off16b".

The input interface of reference clock "cr16" can be switched between LVDS and CML standards using control signal "oncml".

The IC uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal "ce" with frequencies from DC to 17*GHz*. It can also accept a single-ended signal to "cep" or "cen" input with a threshold voltage applied to the other pin. HS CIB can handle a wide range of input signal amplitudes (differential or single-ended). The buffer utilizes on-chip single-ended termination of 50*Ohm* to "vcc" for each input line.

LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a proprietary universal input buffer (UIB) that can run at a frequency up to 1.6*GHz*. The input termination impedance of UIB is controlled by CMOS signal "oncml" and is set to 100*Ohm* differential if "oncml"="0" (true LVDS mode, default state) or 50*Ohm* single-ended to "vcc" if "oncml"="1" (CML mode). Possible input clock application schemes are detailed in Table 2, where Vcm is a common-mode voltage of the clock signal.

Table 2. LS Input Clock Application Schemes.

Interface type	Clock type	"cep" signal			"cen" signal		
		Swing, *mV*	Connection	Vcm, *V*	Swing, *mV*	Connection	Vcm, *V*
LVDS ("oncml" ="0")	Diff.	70-to-500	DC	1.2±1.0	70-to-500	DC	1.2±1.0
	SE	140-to-900	AC	-	Threshold	DC	"vee"-to-"vcc"
		Threshold	DC	"vee"-to-"vcc"	140-to-900	AC	-
CML ("oncml" ="1")	Diff.	70-to-500	DC	"vcc"-Swing/2	70-to-500	DC	"vcc"-Swing/2
			AC	-		AC	-
	SE	140-to-900	AC	-	-	Not connected	-
		140-to-900	AC	-	Threshold	DC	"vcc"
		-	Not connected	-	140-to-900	AC	-
		Threshold	DC	"vcc"	140-to-900	AC	-

As can be seen, UIB is designed to accept differential signals with common mode DC voltages between the negative ("vee") and positive ("vcc") supply rails, as well as AC common mode noise with a frequency up to 5*MHz* and voltage levels from "vee" to "vee"+2.4*V*. It can also receive single-ended signals with a threshold voltage between "vee" and "vcc" applied to the unused pin of the differential input interface.

PLL

The Phase Locked Loop (PLL) contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filter connected between the pins "ftr1" and "ftr2", and two selectable LC-tank voltage-controlled oscillators (VCOs) centered at 8.1*GHz* and 11.8*GHz*. The parameters of the filter schematic components shown in Fig. 2 are for reference only and can be modified based on specific requirements.

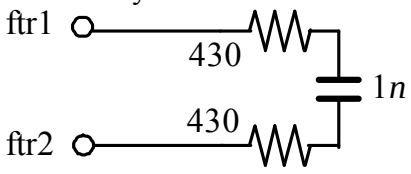

Fig. 2. External Filter Schematic.

PLL is activated by external control signal "offpll"="0" (default state). It can be disabled and converted into a divider by 16 using external signal "offpll"="1".

The main function of PLL is to synthesize full-rate clock "C" by aligning the phase and frequency of the divided clock from internal divider to the externally applied reference clock "cr16". Selection of the required

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VCO is defined by CMOS control signal "off12g": 8.1*GHz* VCO if "off12g"="1" and 11.8*GHz* VCO if "off12g"="0" (default state). The type of the internal clock is defined by CMOS control signal "off16b": divided-by-8 (C8) if "off16b"="1" and divided-by-16 (C16) if "off16b"="0" (default state). The state of the PLL is indicated by output CMOS loss-of-lock alarm signal "lol": "lol"="1" if PLL is not locked, and "lol"="0" if phases and frequencies of internal and reference clocks are matching.

If required, the selected VCO can be externally controlled by voltages applied to pins "ftr1" and "ftr2" as shown in Table 3. In this case, PLL is operating in the open-loop mode. The unused VCO is completely disabled to save power.

Table 3. VCO External Control Modes.

"ftr1" signal, *V*	**"ftr2" signal, *V***	**VCO frequency**
Vccm+0.8=3.1	Vccm=2.3	min
Vccm-0.8=1.5	Vccm=2.3	max
Vccm=2.3	Vccm+0.8=3.1	max
Vccm=2.3	Vccm-0.8=1.5	min

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The divided clocks are supplied to the PLL's phase detector and to clock processor CPR.

CPR

The clock processor (CPR) receives divided clocks from the divider and supplies the selected clock to the low-speed clock output buffer. The type of the clock is defined by CMOS control signal "off16b": divided-by-8 (c8) if "off16b"="1" and divided-by-16 (c16) if "off16b"="0" (default state). The phase of divided-by-16 clock C16 can be altered utilizing the CMOS control pins "phs1" and "phs2" as shown in Table 4.

Table 4. Output Clock Phase Selection.

"phs1"	"phs2"	C16 phase
"vee" (default)	"vee" (default)	0°
"vee"	"vcc"	90°
"vcc"	"vee"	180°
"vcc"	"vcc"	270°

HS COB

The High Speed Clock Output Buffer (HS COB) receives high-speed clock from PLL and converts it into CML output signal "cho" with a frequency up to 17*GHz* and a single-ended CML output swing above 200*mV*. The buffer can be enabled or disabled by the external 2-state control signal "offcho": disabled if "offcho"="1" and enabled if "offcho"="0" (default state).

LS COB

The LVDS Low-Speed Clock Output Buffer (LS COB) receives the signal from CPR and converts it into an LVDS output signal "clo". The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. For the correct operation, it requires external differential 100*Ohm* DC termination at the receiver side. These pins should NEVER be CONNECTED to devices with 50*Ohm* termination to ground WITHOUT DC BLOCKS!

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 5 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed "vee").

Table 5. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Supply Voltage ("vcc")		+3.6	*V*
Power Consumption		0.75	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cep	14	Input	CML differential external clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	13		
chop	17	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to "vcc".
chon	16		
High-Speed I/Os			
cr16p	1	Input	LVDS/CML clock inputs. See LS CIB for allowed application schemes.
cr16n	2		
clop	20	Output	LVDS clock outputs. See LS COB for a detailed description.
clon	19		
Controls			
off16b	4	Input	3.3*V* CMOS control signals.
offcho	5		
off12g	9		
offpll	11		
oncml	21		
phs2	24		
phs1	25		
ftr1	7	-	Pins for connecting the external loop filter. Can be also used for VCO external control in the open-loop mode.
ftr2	8		
lol	6	Output	3.3*V* CMOS control output.

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SUPPLY AND TERMINATION VOLTAGES		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V*)	12, 15, 18, 27-29, 31-39
vee	External ground. (0*V*)	3, 10, 22, 23, 26, 30, 40

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
Ivcc	199		208	*mA*	
Power consumption		670		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Clock (cr16)					
Data Rate	DC		1650	*MHz*	
Swing (SE or Diff.)	140		900	*mV*	Peak-to-peak
CM Voltage Level	"vee"	1.6	"vcc"	*V*	
VCO					
Low frequency, VCO 1		10.8		*GHz*	11.8*GHz* VCO. Active
High frequency, VCO 1		12.7		*GHz*	if "off12g"="0"
Low frequency, VCO 2		7.4		*GHz*	8.1*GHz* VCO. Active
High frequency, VCO 2		8.8		*GHz*	if "off12g"="1"
External control common mode Vccm		2.3		*V*	In the open-loop mode
External control voltage range	Vccm-0.8		Vccm+0.8	*V*	In the open-loop mode
HS Input Clock (ce)					
Frequency	0.0	15	17	*GHz*	
Swing (SE or Diff.)	100		800	*mV*	Peak-to-peak
CM Voltage Level	"vcc"-0.8		"vcc"	*V*	
Duty Cycle	40%	50%	60%		
HS Output Clock (cho)					
Frequency	0.0		17	*GHz*	
Logic "1" level		"vcc"		*V*	
Logic "0" level			"vcc"-0.2	*V*	
Jitter		6		*ps*	Peak-to-peak @12.5*GHz*
Duty Cycle		50%			
LS Output Clock (clo)					
Frequency	0.0	937.5	1063	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS Control Inputs and Outputs					
Logic "1" level	"vcc"-0.4			*V*	
Logic "0" level			"vee"+0.4	*V*	

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PACKAGE INFORMATION

The chip is packaged in a standard 40-pin QFN package shown Fig. 3. Additional package's mechanical information is available on the company's website. It is recommended that the center heat slug located on the back side of the package is soldered to ground to help dissipate heat generated by the chip during operation.

The part's identification label is ASNT8050-PQB. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

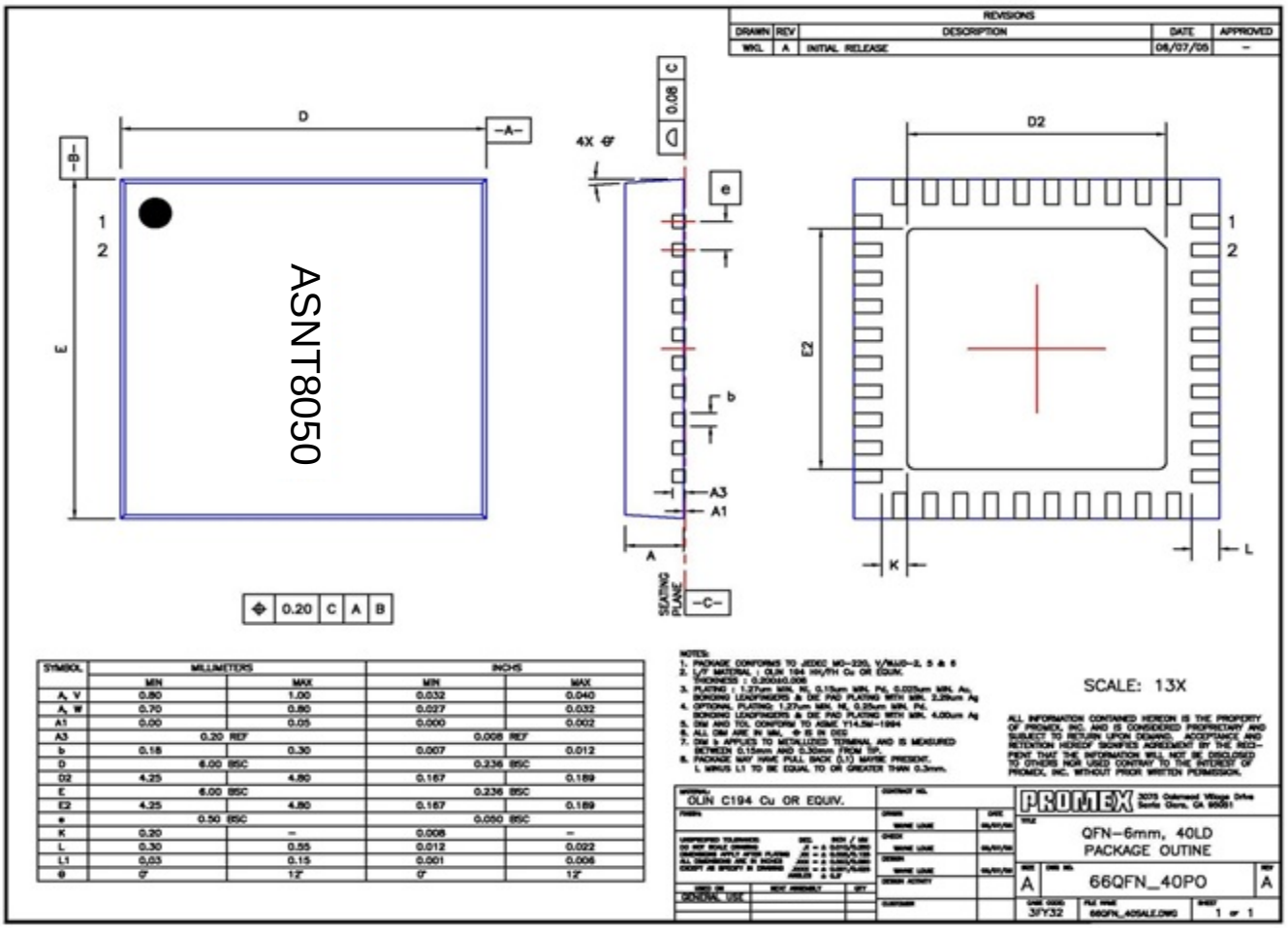

Fig. 3. Package Drawing.

REVISION HISTORY

Revision	Date	Changes
1.1	05-2012	Corrected supply information
1.0	04-2012	First release