ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Sience And Novel Technologies Company, Inc.
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ASNT8140-KMC
23*Gbps* PRBS Generator

- Full length (2^7-1) pseudo-random binary sequence (PRBS) generator.
- Asynchronous reset signal to avoid "all zeros" initial state.
- Additional output delayed by half of sequence period.
- External multiplexing can be used to double the sequence frequency.
- Fully differential input clock and reset buffers with on-chip 50*Ohm* termination.
- Single -3.3*V* power supply.
- Power consumption: 650 *mW*.
- Custom leaded 24-pin metal-ceramic package.

DESCRIPTION

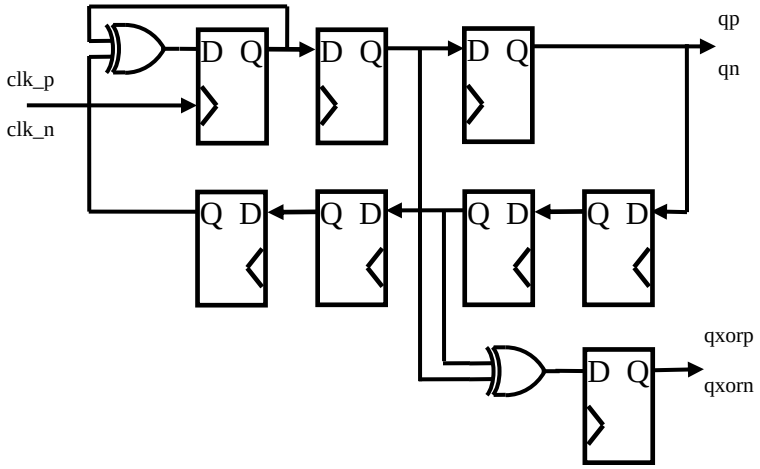

Fig. 1. Functional Block Diagram

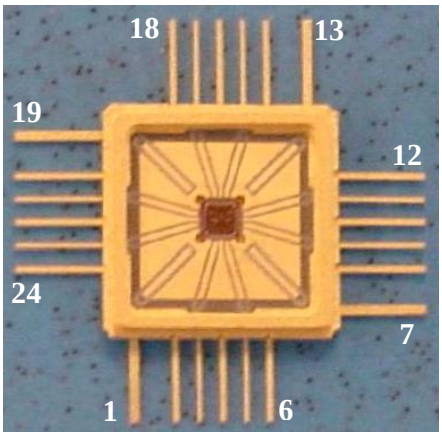

Fig. 2. Package View

The ASNT8140-KMC SiGe IC provides a 127-bit full length pseudo-random binary sequence (PRBS) according to polynomial ($x^7 + x + 1$), where x^D represents a delay of *D* clock cycles. This is implemented with a linear feedback shift register (LSFR) in which the outputs of the seventh and first flip-flops are combined together by XOR function and provided as an input to the first flip-flop of the register. The LSFR based PRBS generator produces 127 binary states, excluding the "all zeros" state. This state is illegal for a XOR-based configuration; it causes LSFR to remain in this state permanently, locking out any further new values from being generated. To prevent this situation, an asynchronous external active-low preset signal ("rstn_p", "rstn_n") is used. When preset is asserted, LSFR is set to the "1000000" state, thus containing at least one "1". When preset is released, the PRBS generator outputs on pins "qp/qn" one bit of a pseudo-random sequence for each clock transition ("clk_p", "clk_n"), starting from the above mentioned state.

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An additional copy (pins "qxorp"/"qxorn") of the same PRBS delayed by 63 bits (half of the sequence period) can be used to increase the frequency of the generated data using an external multiplexing as shown in Fig. 3. The simulated eyes of both signals are shown in Fig. 4.

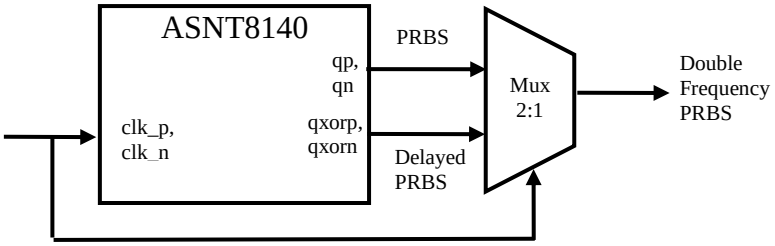

Fig. 3. ASNT8140 Based Double Speed PRBS Generator with 2: l Multiplexor.

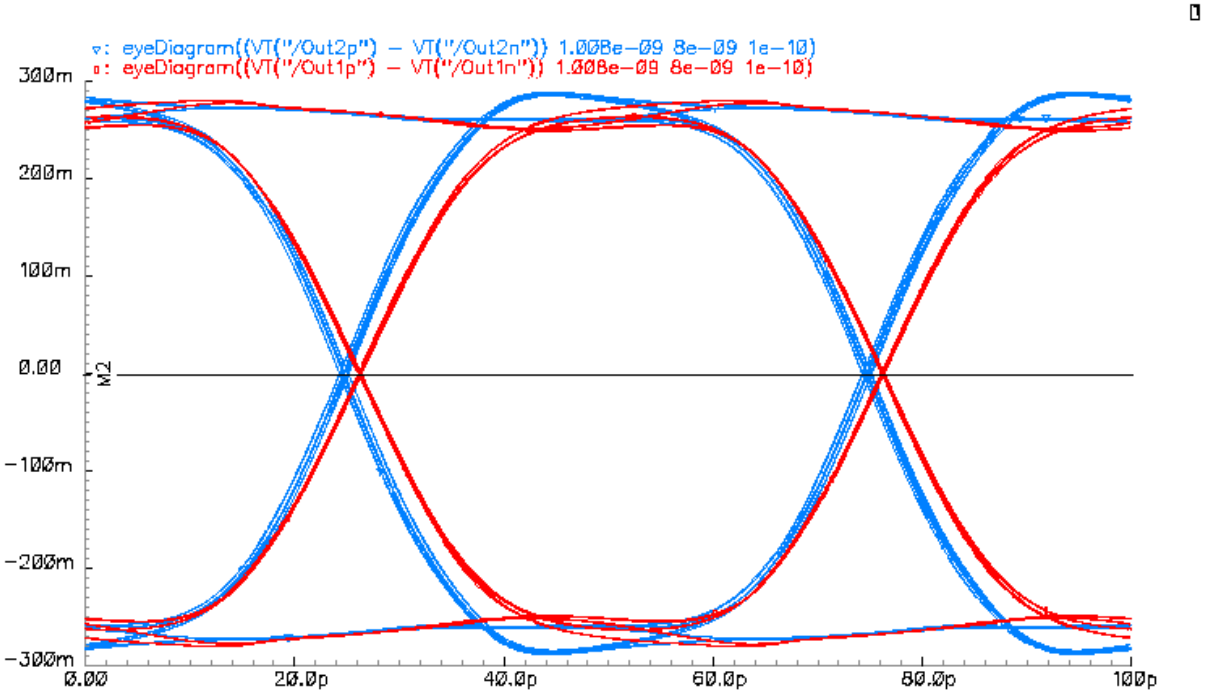

Fig. 4. 20Gbps PRBS Output Eye Diagram (Simulation, Slow Corner, 125°C).

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TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	All even #s	PS	Power Supply: 0V
vee	1,7,13,19	PS	Power Supply: -3.3V
rstn_p	11	Input	Differential CML high-speed asyncronous reset (active low) inputs
rstn_n	9	Input	
clk_p	21	Input	Differential CML high-speed clock signal inputs
clk_n	23	Input	
qp	17	Output	Differential CML high-speed PRBS outputs
qn	15	Output	
qxorn	3	Output	Differential CML high-speed PRBS delayed outputs
qxorp	5	Output	

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		195		mA	
Power		650		mW	
Junction Temp.	-40	25	125	°C	
Input ("rstn")					
Rise time			20%	Clock period	
Recovery time	36			ps	
CM Level	Half of the SE swing				
SE Swing	50	300		mV	Peak-to-peak
Input ("clk")					
Frequency	0.0		23.0	GHz	
CM Level	Half of the SE swing				
SE Swing	50	300		mV	Peak-to-peak
Output ("q")					
CM Level	Half of the SE swing			V	
SE Swing	280	440		mV	Peak-to-peak
Jitter		< 1		ps	Peak-to-peak
Output ("qxor")					
CM Level	Half of the SE swing			V	
SE Swing	280	440		mV	Peak-to-peak
Jitter		2.5		ps	Peak-to-peak

PACKAGE INFORMATION

The chip is packaged into ADSANTEC's custom 24-pin metal-ceramic package (CQFP). The package mechanical information is available on the company's website.

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REVISION HISTORY

Revision	Date	Changes
1.0	8-2011	Initial Release
1.2	1/2012	Updated description Updated Electrical characteristics Table