ADSANTEC
Ultra High-Speed Mixed Signal ASICs
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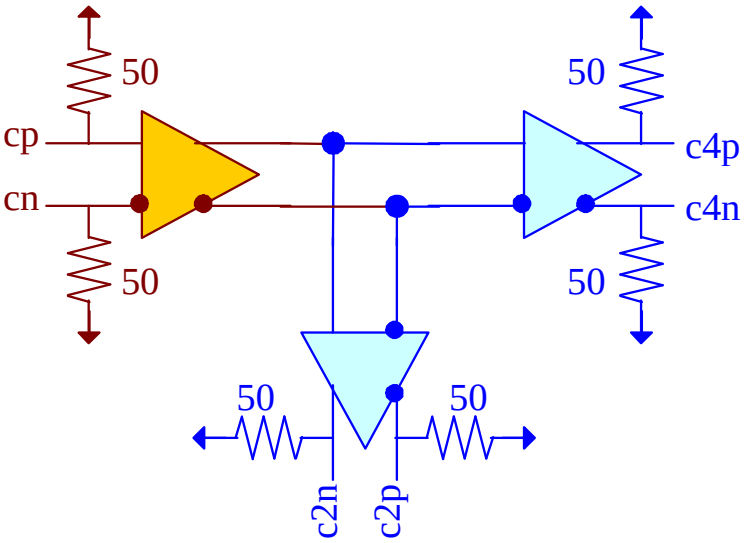
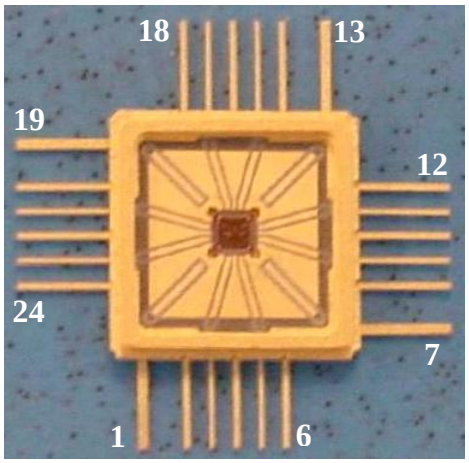
# ASNT8130-KMC
# 32*GHz* Divider by 2 and by 4

- Wide frequency range from DC to 32*GHz*.
- Divided-by-2 and divided-by-4 outputs.
- 50% duty cycle of the divided clock signal.
- Differential or single-ended CML input interface with on-chip 50*ohm* termination to the positive supply rail ("vcc").
- Single ±3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 215*mW* at full operational speed.
- Custom 24-pin metal-ceramic package.

## DESCRIPTION




*Functional Block Diagram*




*Package View*

## DESCRIPTION

ASNT8130-KMC is a high-speed, low-power divider with divided-by-2 and divided-by-4 CML outputs. The divider accepts a CML input clock signal ("cp/cn") with speed from DC to 32*GHz* and provides clean 50% duty cycle divided-by-2 ("c2p/c2n") and divided-by-4 ("c4p/c4n") output signals. The utilized input and output buffers are fully compatible with the CML interface. They feature internal 50*Ohm* termination to the positive supply rail ("vcc") and support both differential (DC or AC) and single-ended (AC) termination modes. The external transmission media can be a printed circuit board or copper coaxial cables with a 50*Ohm* impedance.

ASNT8130-KMC uses a positive 3.3*V* power supply with "vee" as a ground node. It can also operate from a negative 3.3*V* supply voltage with "vcc" as a ground node and the appropriate correction of the control signals. The part may also operate from voltages as low as 2.8*V*, although voltages below 3.1*V* are not recommended. The device is packaged into a custom 24-pin metal-ceramic package.

# TERMINAL FUNCTIONS

| Pin # | Name | Function |
|---|---|---|
| 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24 | vcc | Positive supply node |
| 1, 7, 13, 15, 17, 19 | vee | Negative supply node |
| 23 | cp | Direct clock input |
| 21 | cn | Inverted clock input |
| 3 | c2n | Inverted divided-by-2 clock output |
| 5 | c2p | Direct divided-by-2 clock output |
| 9 | c4n | Inverted divided-by-4 clock output |
| 11 | c4p | Direct divided-by-4 clock output |

# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| **VEE** | -3.1 | -3.3 | -3.5 | *V* | For negative supply |
| **VCC** | 3.1 | 3.3 | 3.5 | *V* | For positive supply |
| **IEE** | | 65 | | *mA* | |
| **Power** | | 215 | | *mW* | |
| **Junction Temp.** | -25 | 50 | 125 | *°C* | |
| **Input** | | | | | |
| Frequency | 0.0 | | 32 | *GHz* | |
| CM Level | Vcc-0.8 | Vcc-0.2 | Vcc | *V* | |
| SE Swing | 50 | 400 | 1000 | *mV* | Peak-to-Peak |
| **Output** | | | | | |
| Frequency (c2p/c2n) | 0.0 | | 16 | *GHz* | Divided-by-2 output |
| Frequency (c4p/c4n) | 0.0 | | 8 | *GHz* | Divided-by-4 output |
| CM Level | Vcc-0.35 | Vcc-0.3 | Vcc-0.25 | *V* | |
| SE Swing | 570 | 600 | 630 | *mV* | Peak-to-Peak |
| Additive Jitter | | TBD | | *ps* | Peak-to-Peak |
| Duty Cycle | | 50% | | | For clock signal |

# PACKAGE INFORMATION

The device is packaged into a custom 24-pin metal-ceramic package. The package's mechanical information is available on the company's website.

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## REVISION HISTORY

| Revision | Date | Changes |
|---|---|---|
| 1.0 | 8-2011 | Initial Release |
| 1.2 | 1/2012 | Updated description<br>Updated Electrical characteristics Table |