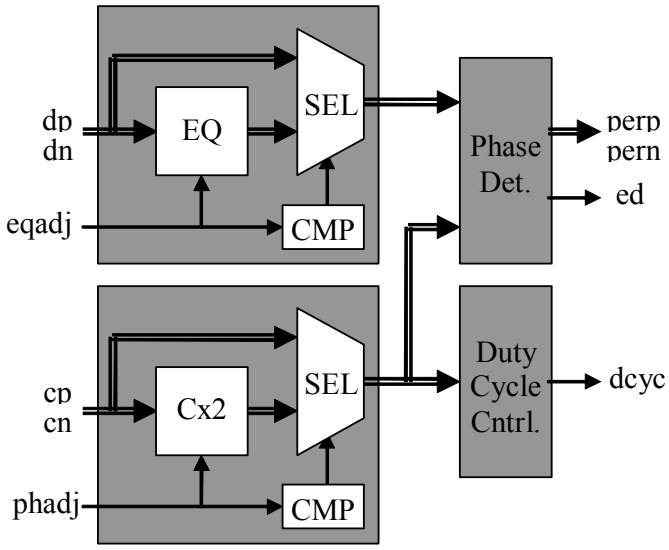
ADSANTEC
Advanced Science and Novel Technology
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

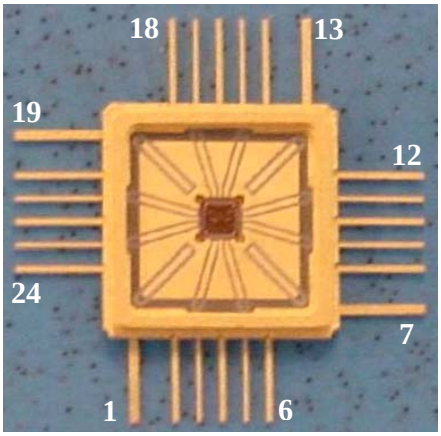
ASNT8120-KMC
28.6G*bps* Linear Phase Detector

- Broadband linear phase detector with differential output.
- Adjustable data input equalizer with a possibility of by-pass.
- Selectable clock multiplier by 2 with externally adjustable duty cycle.
- Clock duty cycle indicator.
- Data edge density indicator.
- Fully differential input data and clock buffers with on-chip 50Ω termination.
- Differential phase error output with on-chip 100Ω termination.
- Single -3.3*V* power supply.
- Power consumption: 750*mW*.
- Custom leaded 24-pin metal ceramic package.

DESCRIPTION



Functional Block Diagram



Package View

The ASNT8120-KMC SiGe IC provides a differential phase error signal "perp"/"pern" that indicates the phase difference between the data "dp"/"dn" bit transitions and the input clock "cp"/"cn". The input data spectrum can be corrected by the equalizer EQ with a frequency response adjustable by the variation of the control input signal "eqadj" within the voltage range from 0 to -2*V*. The lower values of "eqadj" disable the equalizer and send the input data signal directly to the phase detector block (PhaseDet.). The input clock can be delivered to the phase detector block either directly or through the multiplier by 2 (Cx2) with externally adjustable duty cycle. The enabling of the multiplication and value of the duty cycle is controlled by the signal

"phadj" that operates similar to "eqadj" with the same threshold value of -2*V*. The phase detector outputs both the differential phase error signal and the single-ended signal "ed" that delivers an analog voltage indicating the number of transitions in the data bit stream. The additional duty cycle control (DutyCycleCntrl) block delivers the single-ended analog signal "dcyc" that indicates the clock duty cycle deviation from 50%. The detector can process an up to 28.6*Gbps* data and up to 14.3*GHz* clock signals. The part's I/Os support the CML logic interface with on chip 50Ω termination to ground at the input and 100Ω termination to ground at the output. The chip operates from a single -3.3V power supply.

Equalizer

The equalizer frequency response at different values of "eqadj" signal are shown in Fig. 1 and its control characteristic is shown in Fig. 2.

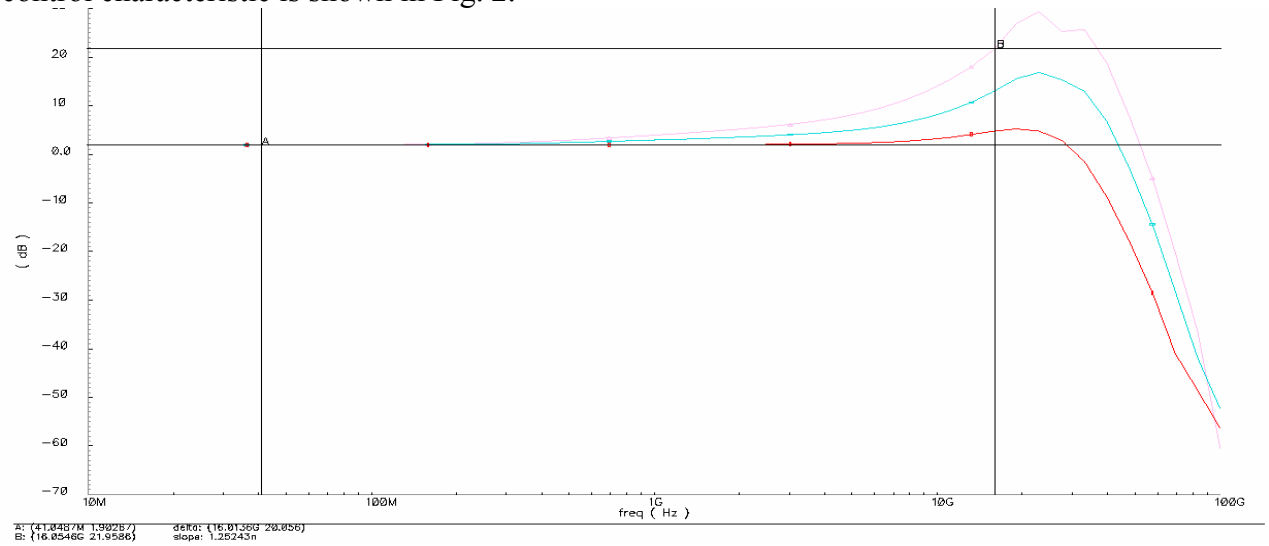


Fig. 1. Equalizer Frequency Response at Full, Half, and No Gain.

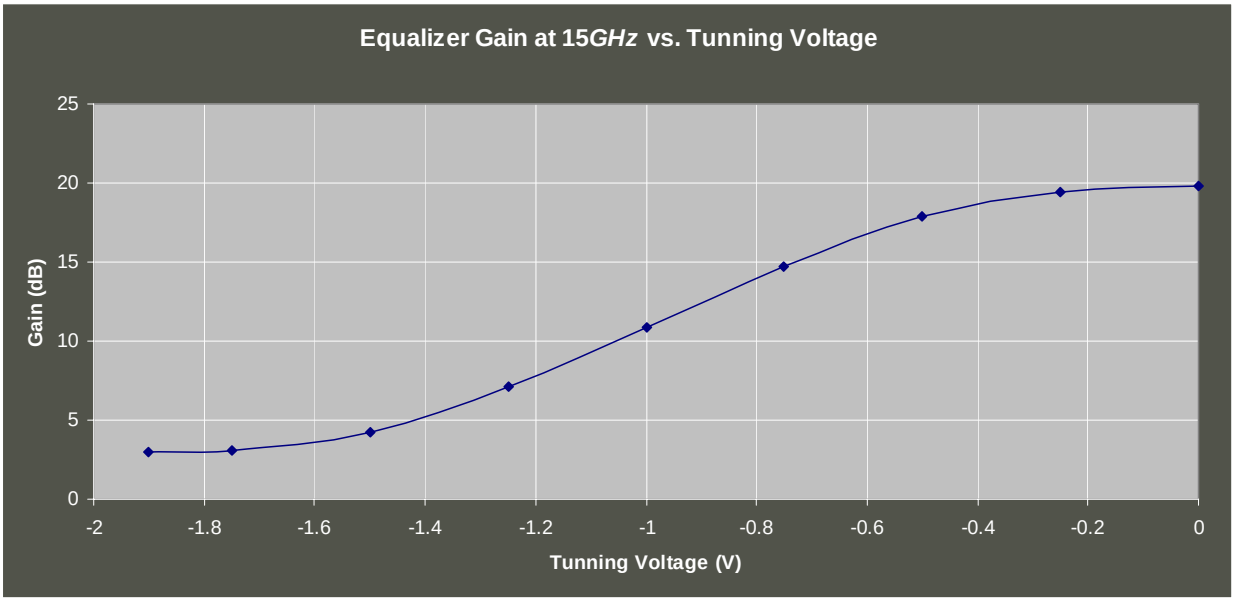


Fig. 2. Equalizer Control Characteristic.

Clock Multiplier

The multiplication by 2 of a 14.3*GHz* input clock is illustrated in Fig. 2 which shows the "dcyc" output voltage vs. the "phadj" input duty cycle control value.

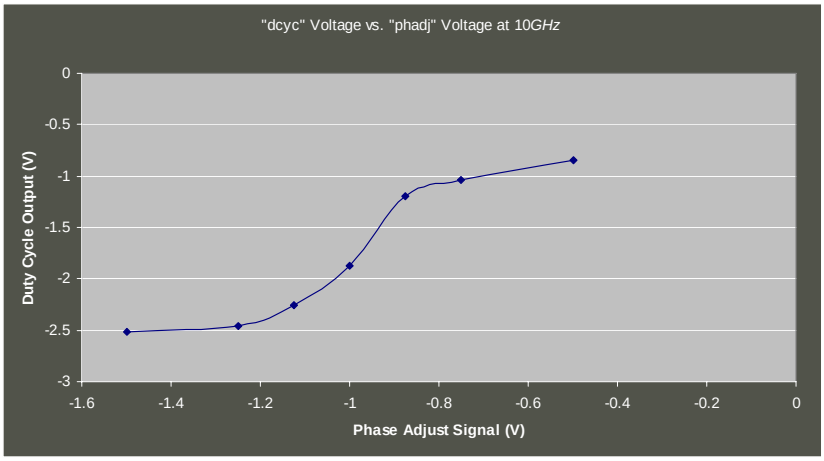


Fig. 3. Duty Cycle Adjustment in the Clock Multiplier.

Phase Detector

The transfer characteristics of the phase detector at 10*Gb/s* and 28.6*Gb/s* data rates are shown in Fig. 3 and Fig. 4 respectively.

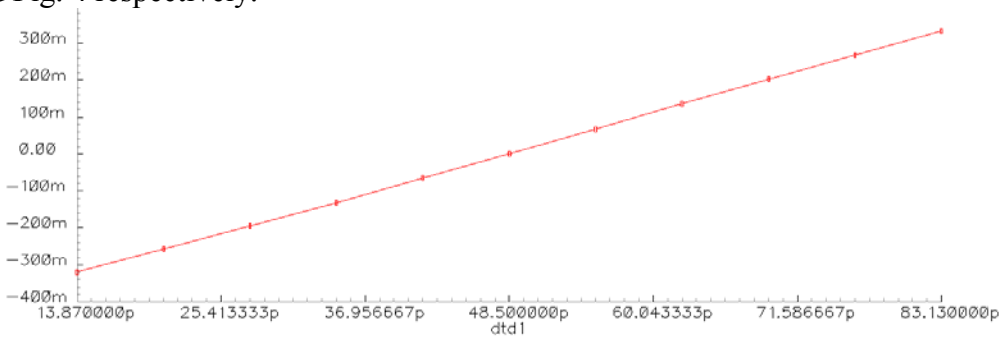


Fig. 4. Phase Detector Characteristic at 10Gb/s Data Rate.

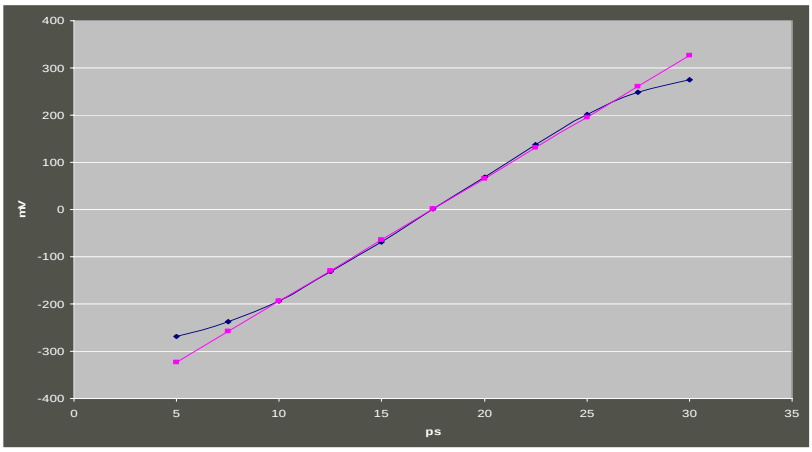


Fig. 5. Phase Detector Characteristic at 28.6Gb/s Data Rate.

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TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	All even #s	PS	Power Supply: 0V
vee	1,13	PS	Power Supply: -3.3V
dp	21	Input	Differential CML high-speed data signal inputs
dn	23	Input	
cp	11	Output	Differential CML high-speed clock signal inputs
cn	9	Output	
perp	17	Output	Phase error output direct
pern	15	Output	Phase error output inverted
eqadj	3	Input	Equalization adjust / by-pass select
dcyc	5	Output	Duty Cycle control output
phadj	7	Input	Clock multiplier delay adjust / by-pass select
ed	19	Output	Edge Density control output

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		230		mA	
Power		750		mW	
Junction Temp.	-25	50	125	°C	
Input (“d”)					
Data rate	0.0		28.6	Gb/s	
CM Level	Half of the SE swing				
SE Swing	10		300	mV	Peak-to-peak
Input (“c”)					
Frequency	0.0		14.3	GHz	
CM Level	Half of the SE swing				
SE Swing	10		300	mV	Peak-to-peak
Output (“per”)					
CM Level		Vcc-0.275		V	
Linear range		300		mV	Single-ended
Tuning Ports (“eqadj” and “phadj”)					
Linear control voltage	-2		0	V	
Switching threshold		-2		V	
Output Indicators (“ed” and “dcyc”)					
Voltage range	-3.3		0.0	V	

PACKAGE INFORMATION

The chip is packaged into the ADSANTEC’s custom 24-pin metal-ceramic package (CQFP). The package mechanical information is available on the company’s website.