ADSANTEC
Ultra High-Speed Mixed Signal ASICs

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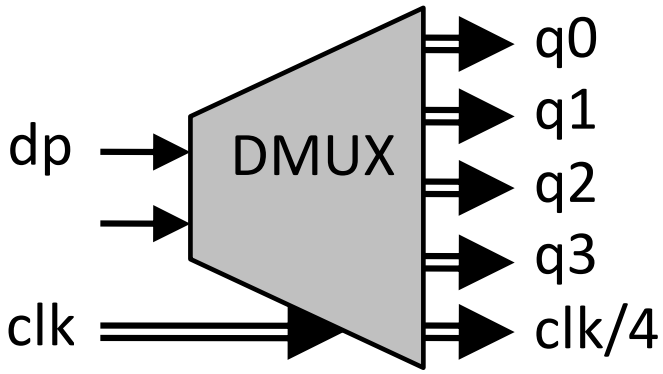
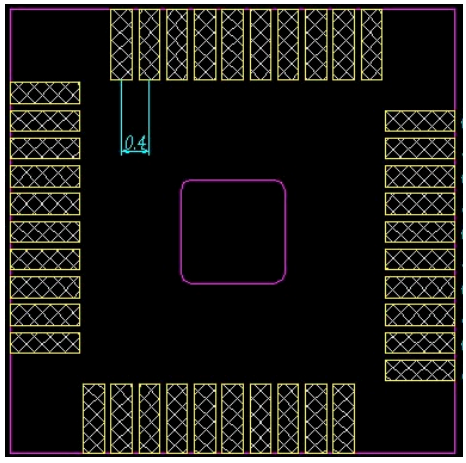
ASNT2121-KMM
50Gb/s 1:4 Digital DMUX

- High speed broadband 1:4 Demultiplexer (DMUX).
- Features a large input clock phase margin (CPM) of over 80%.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Ideal for high speed proof-of-concept prototyping.
- CML compliant I/O data and clock buffers.
- Quarter rate clock output (C/4).
- Single ±3.3*V* power supply.
- Low power consumption of <1.0*W* at 50*Gbps*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 44-pin package.

DESCRIPTION



Functional Block Diagram



Package View

ASNT2121-KMB is a low power and high-speed digital 1 to 4 demultiplexer (DMUX). The DMUX functions seamlessly over data rates (f_{bit}) ranging from DC to 50*Gbps*. The main function of the deserializer is to demultiplex an incoming high speed serial bit stream running at f_{bit} into 4 parallel data channels running at a bit rate of $f_{bit}/4$. Full rate clock must be provided by an external source for the part to function properly. The parallel words are transmitted using CML signaling while a clock divided by 4 is also delivered. The clock and data inputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. All I/O stages are back terminated with on-chip 50*Ohm* resistors. The deserializer uses a single ±3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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POWER SUPPLY CONFIGURATION

The ASNT2121-KMB can operate with either Vcc = 0.0V and Vee = -3.3V or Vcc = +3.3V and Vee = 0.0V. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume Vcc = 0.0*V* and Vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Parameter	Min	Max	Units
Supply Voltage - VEE		-3.8	*V*
Power Consumption		1.0	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Operational Temperature	-5	+85	*°C*
Case Temperature		+100	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL (NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11,12,14, 16,18,20,22,23,25,27,29, 31,33,34,36,38,40,42,44	PS	Power supply: 0*V* (GND)
vee	2, 13, 24, 35	PS	Power supply: -3.3*V*
q0p	30	Output	Differential data output signal
q0n	32		
q1p	37	Output	Differential data output signal
q1n	39		
q2p	41	Output	Differential data output signal
q2n	43		
q3p	4	Output	Differential data output signal
q3n	6		
cep	8	Input	Differential clock input signal
cen	10		
dp	19	Input	Differential data input signal
dn	17		
c4op	26	Output	Differential clock output signal
c4on	28		
n/c	15, 21	-	Not connected

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		280		mA	
Power		924		mW	
Junction Temp.	0	50	125	°C	
Data Input (d0p-d3p) Data Rate	0	10	12.5	Gb/s	
Differential Swing	0.2		0.8	V	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	V	
Clock Input (cep) Frequency	0.0	40	50	GHz	
Differential Swing	0.2		0.8	V	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	V	CM Voltage Level
Duty Cycle	40%	50%	60%		
Data Output (q) Data Rate	0	40	50	Gb/s	
Logic "1" level		V_{CC}		V	
Logic "0" level		V_{CC}-0.45		V	
Jitter		3		ps	Peak-to-peak *@40Gb/s*
Clock Output (c4p) Frequency	0.0	10	12.5	GHz	
Logic "1" level		V_{CC}		V	
Logic "0" level		V_{CC}-0.45		V	
Jitter		2		ps	Peak-to-peak *@10GHz*
Duty Cycle		50%			

PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin metal-ceramic package (CQFP). The dimensioned drawings are included in this document for reference. The package's leads will be trimmed to a length of 1.0mm.

After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   3.9.1 Solderability
   3.2.2 Solder Purity Maintenance

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3.9.2 Solderability Maintenance
3.9.3 Gold Removal

2. The leads will be tinned with Sn63Pb37 solder.

It is recommended that the center heat slug located on the back side of the package *not* be soldered to ground or any other potential to help dissipate heat generated by the chip during operation. For PCB information including footprint etc., please reference the package's associated Gerber file.

The part's identification label is ASNT1121_KMM. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

A date is included in the label of each part. This date allows ADSANTEC to track which parts are from which run lot. The table below gives the lot history of this part and the associated date.

Lot	Date
1	04/10

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.2	11-2011	"Terminal functions" table has been corrected.
1.1	7-2011	Created document