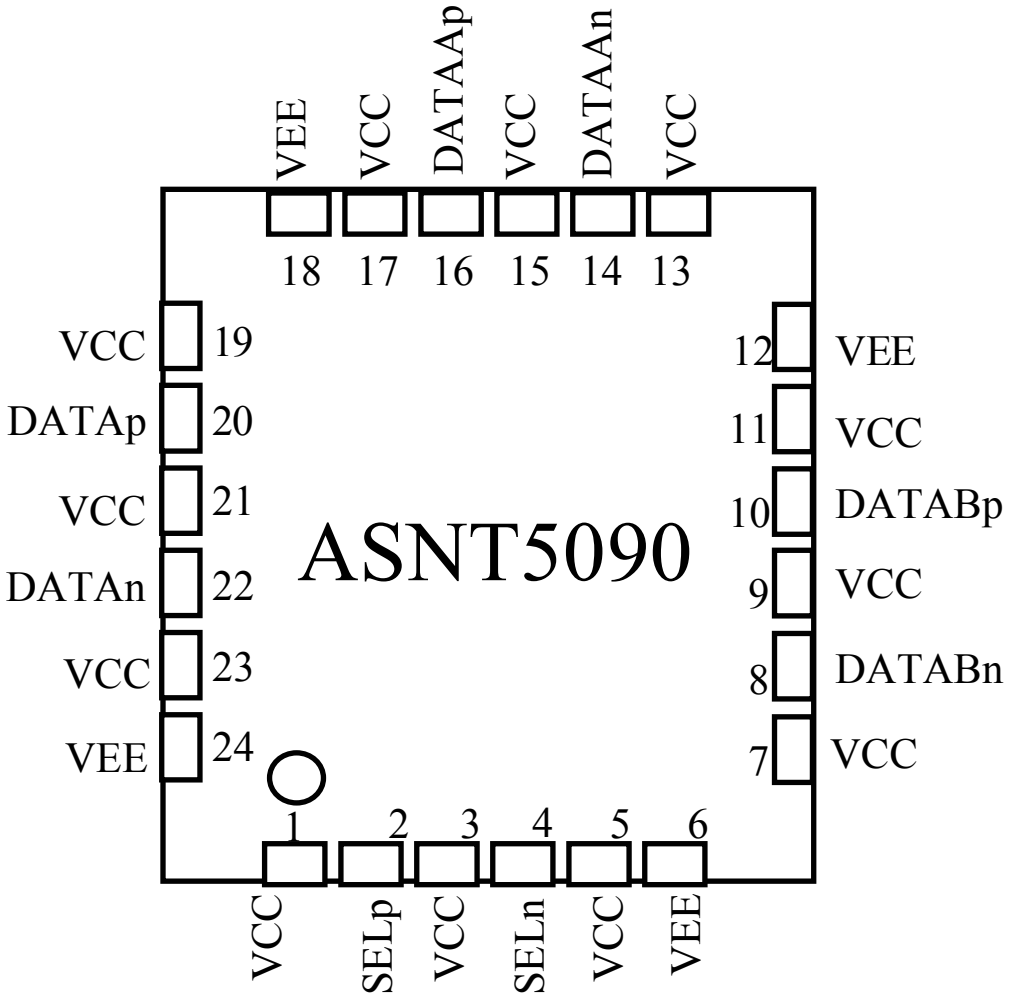
27 Via Porto Grande, Rancho Palos Verdes, CA, 90275. Ph. # 1-310-377-6029. Fax # 1-310-377-9940.

ASNT5090-PQC
17*Gbps* 1:2 Demultiplexer

- High speed broadband 1:2 Demultiplexer gate.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Ideal for high speed proof-of-concept prototyping.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400*mV* single-ended swing.
- Single ±3.3*V* power supply.
- Power consumption: 730*mW*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



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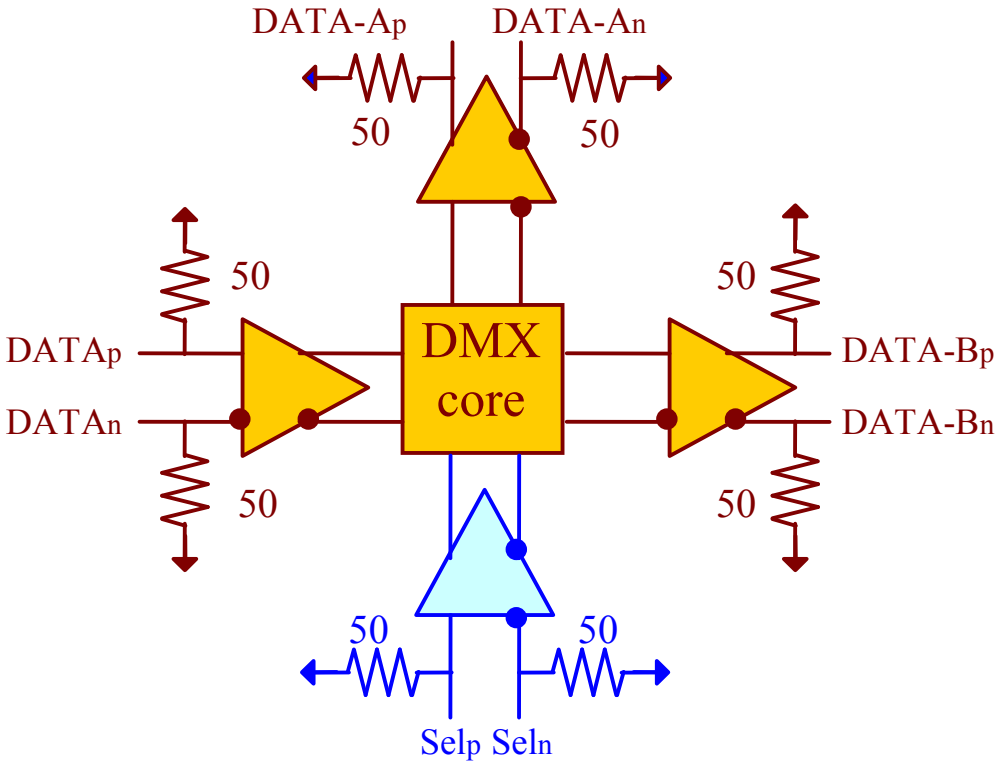
DESCRIPTION

The temperature stable and broadband ASNT5090-PQC SiGe IC can be utilized as a high speed 1:2 demultiplexer (DMX) and is intended for use in high-speed measurement / test equipment. ASNT5090-PQC can receive up a 17*Gbps* input data signal and effectively demultiplex it into two 8.5*Gbps* NRZ output data signals by using an input 8.5*GHz* clock signal on its selector signal inputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single ±3.3V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

NAME	(NO.)		
vcc	1,3,5,7,9,11 13,15,17,19,21,23	PS	Power Supply: 3.3V / 0V
vee	6,12,18,24	PS	Power Supply: 0V / -3.3V
dp dn	20 22	Input	Differential CML high-speed data signal inputs
selp seln	2 4	Input	Differential CML high-speed clock signal inputs
dap dan	16 14	Output	Differential CML high-speed data signal outputs
dbp dbn	10 8	Output	Differential CML high-speed data signal outputs

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	0.0 / -3.3	-3.5	V	±6%
VCC	3.1	3.3 / 0.0	3.5	V	
IEE		220		mA	
Power		730		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d)					
Frequency	0.0		17	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing pk-pk	50	300	800	mV	
Input Clock (sel)					
Frequency	0.0		8.5	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing pk-pk	50	300	800	mV	
Duty Cycle	40%	50%	60%		
Output Datas (da/db)					
Frequency	0.0		8.5	Gbps	
CM Level	Vcc-0.3	Vcc-0.2	Vcc-0.1	V	
SE Swing pk-pk	380	400	420	mV	±5%
Rise/Fall Times (20%-80%)	7	9	11	ps	
Additive Peak-to-Peak Jitter			<1	ps	Input Clock Source Limited

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's website.