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ASNT2112-KMF
1:2 CDR-DMUX

- 1:2 demultiplexer (DMUX) with integrated full-rate CDR (clock and data recovery).
- Supports a wide frequency range digital mode or CDR mode from 21.5*GHz* to 25.6*GHz*.
- Can process RZ and NRZ input data formats.
- Adjustable data time sampling point for optimum BER performance.
- Full rate retimed data output available for 1:1 CDR operation.
- Half rate data outputs support toggle synchronization functionality.
- All output buffers have signal inversion and muting capabilities.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 1.4*W* at 25.6*Gbps*.
- Available in custom leaded 64-pin metal ceramic package.

DESCRIPTION

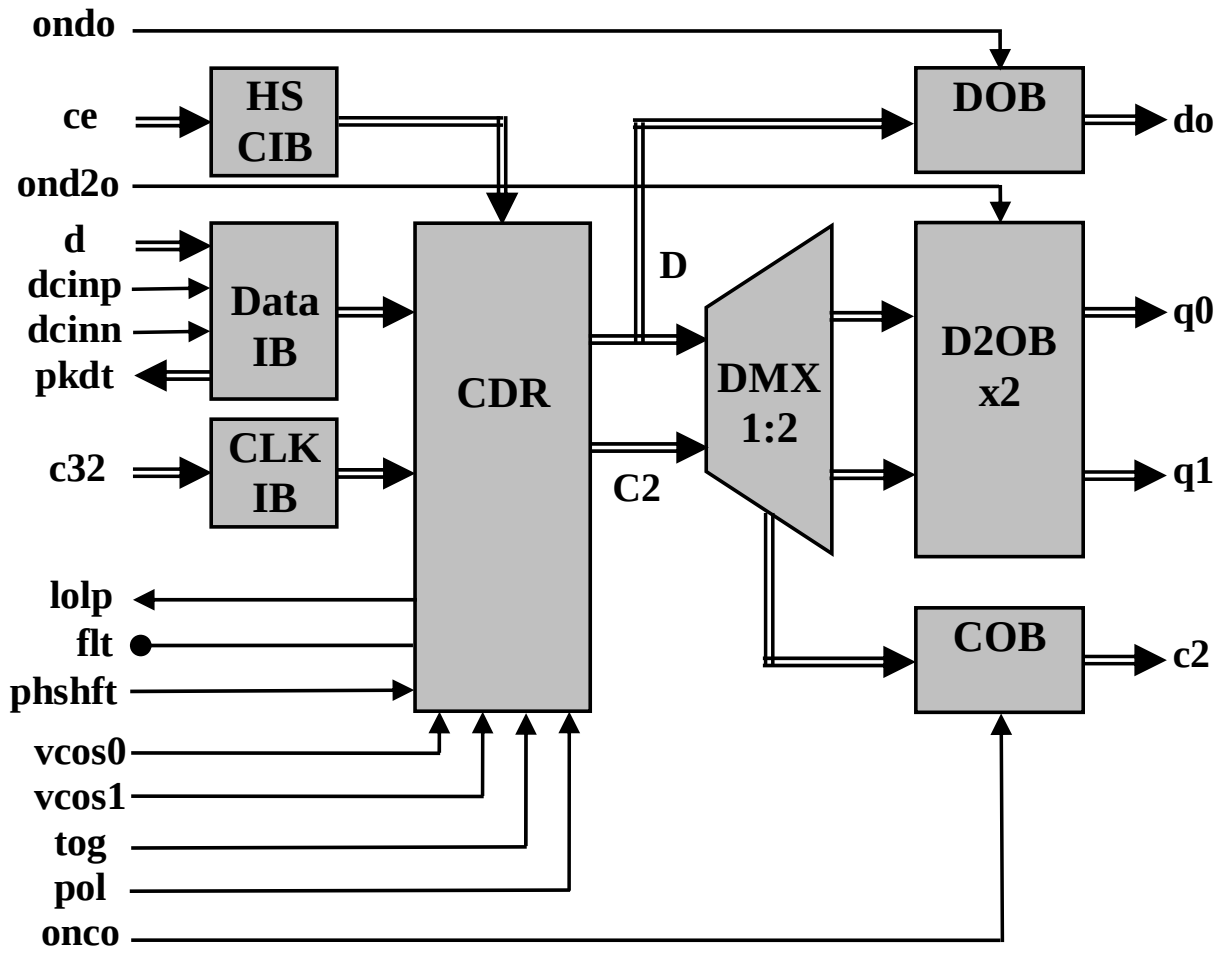

Fig. 1. Functional Block Diagram.

ASNT2112 is a 1:2 deserializer (DMUX) with full rate integrated clock and data recovery (CDR). The DMUX can function at input data rates (f_{bit}) from 21.5*Gbps* up to 25.6*Gbps* by utilizing its multiple on-chip full-rate VCOs or in a broadband (DC to 25.6*Gbps*) digital mode. An external full clock "ce" must be applied to the high speed clock input buffer (HS CIB) for digital operation. Selection of the desired working data rate and mode is accomplished through pins "vcos0" and "vcos1" (see the Table in CDR section below).

The main function of ASNT2112 is to demultiplex a serial input data channel "d" running at a bit rate of f_{bit} into 2 parallel NRZ data channels "q0" and "q1" running at bit rates of $f_{bit}/2$. A full rate retimed NRZ data output signal "do" is made available through the data output buffer (DOB) allowing ASNT2110 to be used as a 1:1 CDR. Half rate clock "c2" is supplied with tight phase alignment to the two demultiplexed data outputs through the clock output buffer (COB).

The high sensitivity data input buffer (Data IB) in unison with the CDR ensures accurate clock and data recovery for input data signals in either the RZ or NRZ format with amplitudes greater than 50*mV* peak to peak (p-p) differential or single-ended. This is accomplished with a combination of Data IB having high gain while delivering 30*GHz* of analog bandwidth and the CDR circuitry incorporating both a phase and frequency acquisition loop to recover a full rate clock from the input data stream. This recovered clock is used to sample the input data bits before they are demultiplexed while its phase can be adjusted externally through pin "phshft" to locate the optimum sampling point to achieve the lowest system bit error rate. The application of an external low speed system clock "c32" running at 1/32 the frequency of the active VCO is required for CDR to operate correctly.

Data IB is a high-speed differential CML buffer providing on-chip 50*Ohm* termination and is designed to be driven by devices with 50*Ohm* source impedance. The threshold tuning pins "dcinp/n" provide proper offset adjustment when the buffer is operating with single ended input signaling. A peak detector is also included to provide means of demodulating any AM components carried by "d" that range in frequency up to a few hundred *KHz*. Results of the peak detector are delivered by the differential signal "pkdt".

The low speed clock input buffer (CLK IB) accepts the system reference clock "c32" through a fully LVDS compliant interface and delivers it to CDR. All output buffers provide CML signaling and are back terminated with 50*Ohms*. DOB, COB, and the two half rate data output buffers (D2OBx2) can be individually diabled through pins "ondo", "onco", and "ond2o" to save power.

Utilizing pin "pol", the deserializer can invert the polarity of the three output data signals. Pin "tog" flips the order of "q0" and "q1" thus simplifying the interface between ASNT2112 and a following ASIC. It also can function as a way to synchronize the bit order of two or more ASNT2112s working in parallel.

A loss of lock 2.5*V* CMOS alarm signal "lolp" is generated by CDR. Off chip passive filter components are required by CDR and are connected through the pin "ftr".

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −5°*C* to 125°*C* of junction temperature. Its temperature resistance is 15°*C* /*W*.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal "d" with bit rates up to 25.6*Gbps* in either the RZ or NRZ format due to its 30*GHz* of analog bandwidth. It can also accept a single-ended signal to one of its input ports "dp" or "dn" with a threshold voltage applied to the opposite tuning pin "dcinn" or "dcinp". The tuning pins have input impedances of 1*KOhm* and allow the user to change the slicing level before the data is sampled by the recovered clock. A tuning voltage from positive (Vcc) to negative (Vee) supply rail delivers Vcc-150*mV* of input port DC voltage shift. Data IB can handle input signal amplitudes between 50*mV* and 600*mV* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to Vcc for each input line.

Also included in Data IB is an input signal peak detector that delivers its response through the output differential signal "pkdt". The detector can demodulate AM component(s) carried by the input data stream that are in the frequency range of up to a few hundred *kHz*. The peak detector's output impedance is 4*KOhm* single ended to Vcc.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal "ce" with frequencies from 10*MHz* to 31*GHz*. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. HS CIB can handle input signal amplitudes between 200*mV* and 1.2*V* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to Vcc for each input line.

CLK IB

The Clock Input Buffer (CLK IB) consists of a proprietary universal input buffer (UIB) that exceeds the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals running at frequencies up to 1*GHz* with amplitudes higher than 60*mV* p-p, DC common mode voltage variation between Vcc and Vee, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes of more than 60*mV* p-p and threshold voltages between Vcc and Vee. The input termination impedance is set to 100*Ohm* differential.

CDR

The Clock and Data Recovery Block (CDR) contains both a phase and frequency acquisition loop that require a single off-chip filter connected to the pin "ftr". The frequency loop works in concert with "c32" while the phase loop utilizes "d".

The main function of CDR is to frequency lock the on-chip active VCO to the input data signal (clock recovery) while phase aligning it to latch in the incoming data with minimal error (data recovery). By default, CDR aligns the recovered clock's working edge in the middle of the incoming data bits. Pin "phshft" can be utilized to shift this position from one edge of the data bit to the other (±30*ps*) in order to locate the optimum sampling point to generate the lowest system BER. The recovered clock is divided down in frequency by two "C2" and utilized by DMX 1:2 to demultiplex the recovered data.

By utilizing the CMOS control pins "vcos0" and "vcos1", the desired working frequency of CDR can be selected in accordance with the table below.

"vcos0"	"vcos1"	VCO Center Frequency (*GHz*)
0V	0V	21.5
0V	2.5	23.1
2.5	0V	25.6
2.5 (default)	2.5 (default)	Digital Mode

The lock detect circuitry signals an alarm through the CMOS signal "lolp" when a frequency difference exists between the applied system reference clock "c32" and recovered full rate clock divided-by-32 that is greater than ±1000*ppm*.

Another feature included in CDR is the ability to simultaneously invert the polarity of all three data outputs through CMOS input pin "pol" ("pol"=1 (default), direct; "pol"=0, inverted). The half rate output data streams can be switched by using the CMOS input pin "tog". "tog" provides a means to synchronize two adjacent ASNT2112s operating in parallel. The synchronization process may be accomplished by the "blind" toggling of a single ASNT2112 and leaving the task of recognizing the "right" position by downstream components (e.g. FEC chip).

DMX1:2

The 1 to 2 Demultiplexer (DMX1:2) latches in the retimed data stream "D" from CDR on both edges of the half rate clock signal "C2". The high speed data signal is subsequently demultiplexed into two half rate NRZ data signals and delivered to D2OBx2 in parallel fashion as 2-bit wide words running at a data rate up to 12.8*Gbps*.

DOB

The Data Output Buffer (DOB) receives the full rate retimed serial data stream "D" from CDR and converts it into the CML output signal "do" with a single ended swing of 400*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 25.6*Gbps*. The buffer can be enabled or disabled by the external 2-state CMOS control signal "ondo". The logic "0" state disables the buffer completely to save power while the logic "1" state (default) provides a full rate data output.

D2OBx2

The Half Rate Data Output Buffer (D2OBx2) receives two half rate data signals from DMX1:2 and converts them into CML output signals "q0" and "q1" with single ended swings of 400*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 12.8*Gbps*. The buffer can be enabled or disabled by the external 2-state CMOS control signal "ond2o". The logic "0" state disables the buffer completely to save power while the default logic "1" state (default) provides the two half rate data outputs.

COB

The Clock Output Buffer (DOB) receives a half rate clock signal from DMX1:2 and converts it into the CML output signal "c2" with a single ended swing of 400*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 12.8*GHz*. The buffer can be enabled or disabled by the external 2-state CMOS control signal "onco". The logic "0" state disables the buffer completely to save power while the logic "1" state (default) provides a half rate clock output. COB is designed so "c2"'s negative edge is aligned to the half rate output data crossing points.

Absolute Maximum Ratings

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Parameter	**Min**	**Max**	**Units**
Supply Voltage - VCC		+3.6	*V*
Power Consumption		1.53	*W*
Operational Temperature	-5	+70	*ºC*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

Terminal Functions

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
cep	3	Input	CML differential full rate clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	5		
q1p	21	Output	CML differential half rate data outputs. Require external SE 50*Ohm* termination to "vcc".
q1n	19		
q0p	30		
q0n	28		
c2p	37	Output	CML differential half rate clock outputs. Require external SE 50*Ohm* termination to "vcc".
c2n	35		
dop	46	Output	CML differential full rate data outputs. Require external SE 50*Ohm* termination to "vcc".
don	44		

dp	56	Input	CML differential data inputs with internal SE 50*Ohm* termination to "vcc".
dn	58		
Low-Speed I/Os			
c32p	12	Input	LVDS clock inputs.
c32n	14		
pkdtp	51	Output	Peak detector outputs.
pkdtn	52		
Controls			
vcos1	7	LS In., CMOS	Select CDR or digital mode. Select VCO frequency in CDR mode.
vcos0	10		
ftr	8	I/O	External CDR filter connection.
lolp	25	LS Out, CMOS	CDR lock indicator (high: no lock; low: locked).
ond2o	26	LS IN, CMOS	D2OBx2 control (active: low, buffer is disabled; default: high, buffer is on).
onco	39	LS IN, CMOS	COB control (active: low, buffer is disabled; default: high, buffer is on).
tog	40	LS IN, CMOS	D2OBx2 output signal order flip (default: high; active: low).
pol	41	LS IN, CMOS	Data output signal polarity flip (default: high, inverted data outputs; active: low, direct data outputs).
ondo	42	LS IN, CMOS	DOB control (active: low, buffer is disabled; default: high, buffer is on).
dcinp	53	LS IN	DATA IB thresholding.
dcinn	61		
phshft	62	LS IN	CDR sampling point adjustment (±30ps).

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3*V*)	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60.
vee	Negative power supply. (GND or 0*V*)	1, 16, 17, 32, 33, 48, 49, 50, 63, 64.
nc	Unconnected pin.	9, 23, 24.

ELECTRICAL CHARCTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
		General Parameters			
V_{CC}	+3.0	+3.3	+3.6	*V*	±9%
V_{EE}		0.0		*V*	
Power Consumption		1.40	1.53	*W*	
Junction Temperature	-25	50	125	*°C*	
		HS Input Data (d)			
Data Rate	DC		25.6	*Gbps*	RZ or NRZ
Swing p-p (Diff or SE)	0.05		0.6	*V*	
Common Mode Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
		LS Input Reference Clock (c32)			
Frequency	671.875		800	*MHz*	
Swing p-p (Diff or SE)	0.06		0.8	*V*	
Common Mode Voltage Level	V_{EE}		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
		HS Output Full Rate Data (do)			
Data Rate	DC		25.6	*Gbps*	NRZ
Logic "1" level		V_{CC}		*V*	
Logic "0" level		V_{CC}-0.4		*V*	
Jitter		8		*ps*	p-p @ 25.6*Gbps*
		HS Output Half Rate Data (q0,q1)			
Data Rate	DC		12.8	*Gbps*	NRZ
Logic "1" level		V_{CC}		*V*	
Logic "0" level		V_{CC}-0.4		*V*	
Jitter		7		*ps*	p-p @ 12.8*Gbps*
		HS Output Half Rate Clock (CDR Mode) (c2)			
Data Rate	10.75		12.8	*GHz*	
Logic "1" level		V_{CC}		*V*	
Logic "0" level		V_{CC}-0.4		*V*	
Jitter		5		*ps*	p-p @ 12.8*GHz*
		Input Data Buffer Thresholds (dcin)			
Input DC Voltage	Vee		Vcc	*V*	
Input Data Channel Voltage Shift	0		150	*mV*	Referenced to Vcc
		Output of Peak Detector (pkdt)			
Swing p-p (Diff)	-1		1	*V*	Over full input range
Common Mode Voltage Level		Vcc-1.0		*V*	
		Input Sampling Point Adjustment (phshft) optional			
Input DC Voltage	Vcc-1.0	NC	Vcc	*V*	NC=Not Connected

Phase Shift	-15	0	+15	*ps*	
Shift Stability vs. Temperature (0-125°C)	-2		2	ps	< ±10%
Bandwidth	0.0		100	*MHz*	
CMOS Control Inputs/Outputs					
Logic "1" level	V_{CC}-0.4			*V*	
Logic "0" level			V_{EE}+0.4	*V*	
Timing Parameters					
"c2" to "q0 & q1" delay variation		2		*ps*	Over the full temperature range

PACKAGE INFORMATION

The chip die is housed in a custom, 64-pin Kyocera metal-ceramic package (CQFP). Kyocera's dimensioned drawings are included in this document for reference. The package's leads shall be trimmed to length as specified in Figure 2.

After trimming, the package's leads shall be further processed as follows:

1. The lead's gold plating shall be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal

2. The leads shall be tinned with Sn63Pb37 solder.

The part's identification label is ASNT2112_KMF. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

A date is included in the label of each part. This date allows ADSANTEC to track which parts are from which run lot. The table below gives the lot history of this part and the associated date.

Lot	Date
1	02/09
2	12/09

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.6	6-2010	Added additional packaging information Changed package image in Figure 2
1.5	4-2010	Added case temperature
1.4	2-2010	Added absolute maximums rating table Replaced TBDs with values Added RoHS compliancy Added revision history table Revised VCO table Added packaging diagram
1.3	12-2009	Adjusted block diagram Updated center frequencies in VCO table Updated external filter pin assignments Revised packaging information section
1.2 Previous release Rev 1.1 2-2009	4-2009	Updated center frequencies in VCO table Updated power consumption value