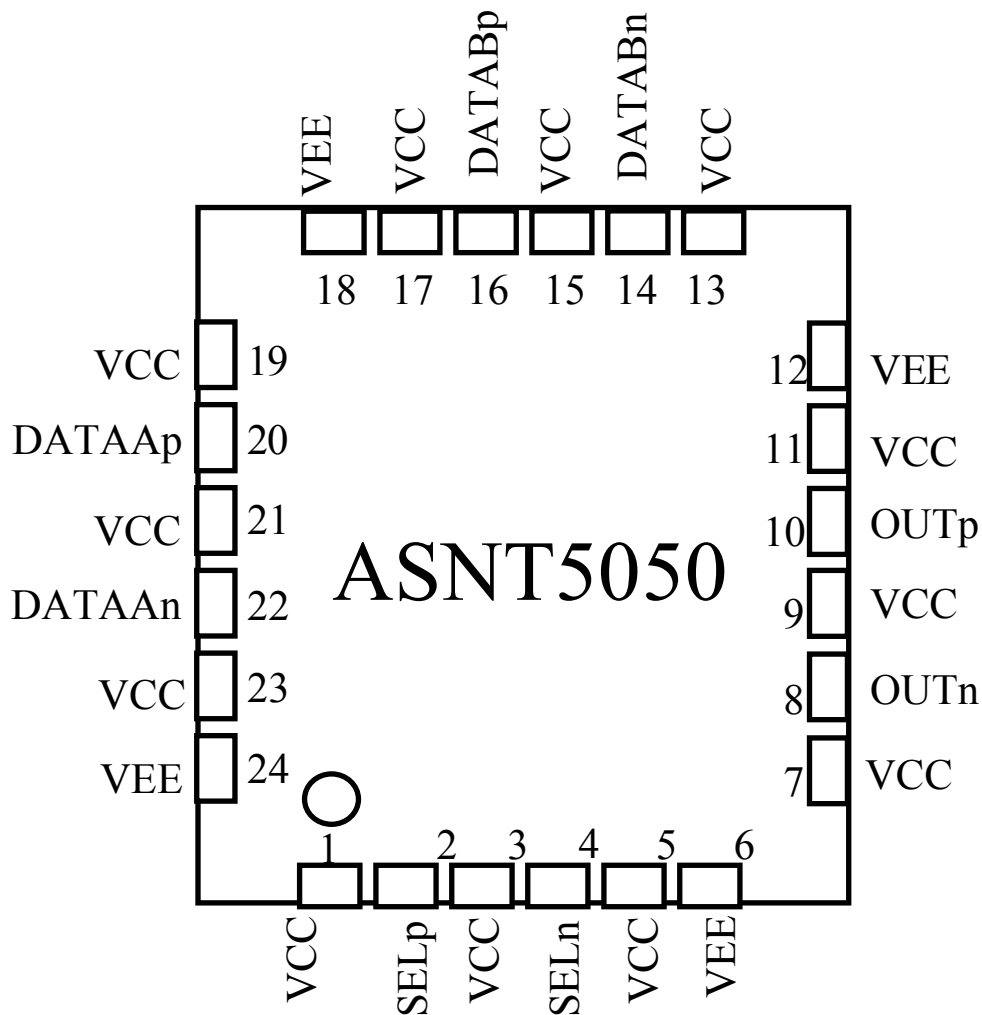


ASNT5050-PQC 17Gbps 2:1 Multiplexer

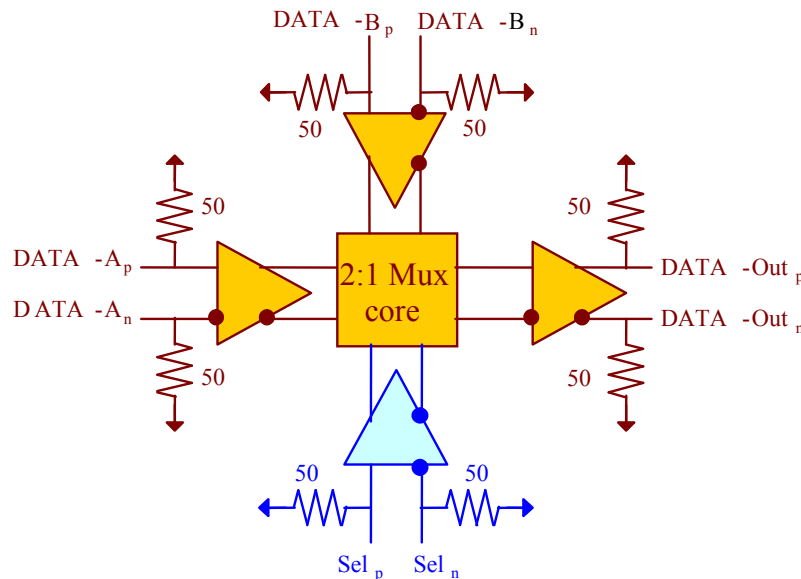
- High speed broadband 2:1 Multiplexer/Selector (MUX) gate.
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Ideal for use as a selector switch or as a high speed 2:1 multiplexer.
- Fully differential input and output buffers with on-chip 50Ω termination.
- CML output interface with 400mV single-ended swing.
- Single -3.3V power supply.
- Power consumption: 450mW.
- Fabricated in SiGe for high performance, yield, and reliability.
- Standard MLF/QFN 24-pin package.



DESCRIPTION

The temperature stable and broadband ASNT5050-PQC SiGe IC can be utilized as either a selector switch or a high speed 2:1 multiplexer (MUX) and is intended for use in high-speed measurement / test equipment. When employed as a selector switch, ASNT5050-PQC can route one of its up to 17Gbps data inputs to its output while effectively blocking the other data input. Selection of a specific data input is achieved through appropriate external biasing of the selector signal inputs. As a 2:1 MUX, ASNT5050-PQC can receive up to 8.5Gbps input data signals and effectively multiplex them into a 17Gbps NRZ output data signal by using an input 8.5GHz clock signal on its selector signal inputs. The part's I/Os support the CML logic interface with on chip 50Ω termination and may be used differentially, AC/DC coupled, single-ended, or in any combination. It operates from a single -3.3V power supply.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	(NO.)	TYPE	DESCRIPTION
vcc	1,3,5,7,9,11	PS	Power Supply: 0V
vee	6,12,18,24	PS	Power Supply: -3.3V
dap	20	Input	Differential CML high-speed data signal inputs
dan	22		
dbp	16	Input	Differential CML high-speed data signal inputs
dbn	14		
selp	2	Input	Differential CML high-speed clock signal outputs
seln	4		
outp	10	Output	Differential CML high-speed data signal outputs
outn	8		



ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		135		mA	
Power		450		mW	
Junction Temp.	-25	50	125	°C	
Input Data (d)					
Data rate	0.0		17	Gbps	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Input Clock (sel)					
Frequency	0.0		10	GHz	
CM Level	Vcc-0.8	Vcc-0.3	Vcc+0.3	V	
SE Swing	50	300	800	mV	Peak-to-Peak
Duty Cycle	40%	50%	60%		
Output Data (out)					
Data rate	0.0		17	Gbps	
CM Level	Vcc-0.3	Vcc-0.2	Vcc-0.1	V	
SE Swing	380	400	420	mV	Peak-to-Peak
Rise/Fall Times	7	9	11	ps	20%-80%
Additive Jitter			<1	ps	Peak-to-Peak

PACKAGE INFORMATION

The chip is packaged in a standard 24-pin QFN package. The package's mechanical information is available on the company's [website](#).