ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Sience And Novel Technologies Company, Inc.
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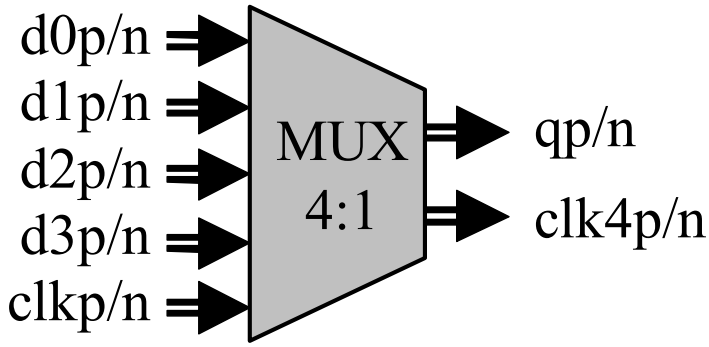
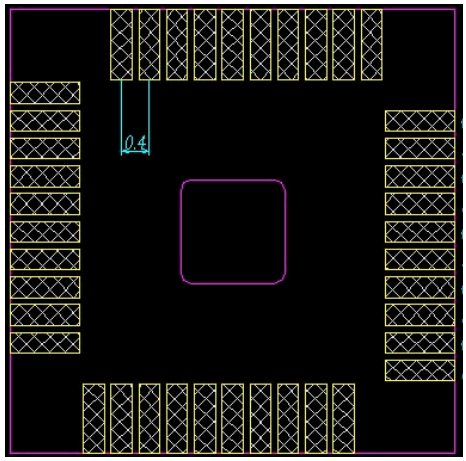
ASNT1121-KMM
50Gb/s 4:1 Digital MUX

- High speed broadband 4:1 Multiplexer (MUX).
- Exhibits low jitter and limited temperature variation over industrial temperature range.
- Ideal for high speed proof-of-concept prototyping.
- Differential CML I/O data and clock buffers.
- Quarter-rate clock output.
- Single ±3.3*V* power supply.
- Low power consumption of <1.0*W* at 50*Gbps*.
- Fabricated in SiGe for high performance, yield, and reliability.
- Custom CQFP 44 pin package.

DESCRIPTION



Functional Block Diagram



Package Layout

ASNT1121-KMB is a low power and high-speed digital 4 to 1 serializer-multiplexer (MUX). The MUX functions seamlessly over data rates (f_{bit}) ranging from DC to 50*Gbps*. The main function of the part is to multiplex 4 parallel differential CML data signals running at a bit rate of $f_{bit}/4$ into a high speed serial bit stream running at a bit rate of f_{bit}. Differential or single-ended full-rate clock must be provided by an external source for the part to function properly. The serialized data words and clock divided by 4 are transmitted through CML output interfaces. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. All I/O stages are back terminated with on-chip 50*Ohm* resistors. The serializer uses a single ±3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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POWER SUPPLY CONFIGURATION

The ASNT1121-KMC can operate with either Vcc = 0.0V and Vee = -3.3V or Vcc = +3.3V and Vee = 0.0V. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume Vcc = 0.0*V* and Vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground.

Parameter	**Min**	**Max**	**Units**
Supply Voltage - VEE		-3.8	*V*
Power Consumption		1.0	*W*
RF Input Voltage Swing (SE)		1.4	*V*
Operational Temperature	-5	+85	*°C*
Case Temperature		+100	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL		**TYPE**	**DESCRIPTION**
NAME	**(NO.)**		
vcc	1,3,5,7,9,11,12,14, 16,18,20,22,23,25,27,29, 31,33,34,36,38,40,42,44	PS	Power supply: 0*V* (GND)
vee	2, 13, 24, 35	PS	Power supply: -3.3*V*
d0p d0n	30 32	Input	Differential quarter-rate data input signals with internal 50*Ohm* termination.
d1p d1n	37 39	Input	Differential quarter-rate data input signals with internal 50*Ohm* termination.
d2p d2n	41 43	Input	Differential quarter-rate data input signals with internal 50*Ohm* termination.
d3p d3n	4 6	Input	Differential quarter-rate data input signals with internal 50*Ohm* termination.
cep cen	8 10	Input	Differential full-rate clock input signals with internal 50*Ohm* termination.
qp qn	19 17	Output	Differential full-rate data output signals. Require external 50*Ohm* termination.
c4op c4on	26 28	Output	Differential clock divided-by-4 output signals. Require external 50*Ohm* termination.
n/c	15, 21	-	Not connected

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VEE	-3.1	-3.3	-3.5	V	±6%
VCC		0.0		V	
IEE		290		mA	
Power		960		mW	
Junction Temp.	0	50	125	°C	
Data Input (d0p-d3p) Data Rate	DC	10	12.5	Gb/s	
Differential Swing	0.2		0.8	V	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	V	
Clock Input (cep) Frequency	DC	40	50	GHz	
Differential Swing	0.2		0.8	V	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	V	CM Voltage Level
Duty Cycle	40%	50%	60%		
Data Output (q) Data Rate	DC	40	50	Gb/s	
Logic "1" level		V_{CC}		V	
Logic "0" level		V_{CC}-0.6		V	
Jitter		3		ps	Peak-to-peak *@40Gb/s*
Clock Output (c4p) Frequency	DC	10	12.5	GHz	
Logic "1" level		V_{CC}		V	
Logic "0" level		V_{CC}-0.6		V	
Jitter		2		ps	Peak-to-peak *@10GHz*
Duty Cycle		50%			

PACKAGE INFORMATION

The chip die is housed in a custom, 44-pin metal-ceramic quad flat package (CQFP). The package dimensioned drawings are included in this document for reference. The package leads will be trimmed to a length of 1.0mm.

After trimming, the package leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal

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2. The leads will be tinned with Sn63Pb37 solder.

It is recommended that the center heat slug located on the back side of the package *not* be soldered to ground or any other potential to help dissipate heat generated by the chip during operation. For PCB information including footprint etc., please reference the package's associated Gerber file.

The part's identification label is ASNT1121_KMM. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

A date is included in the label of each part. This date allows ADSANTEC to track which parts are from which run lot. The table below gives the lot history of this part and the associated date.

Lot	Date
1	04/10

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
1.3	11-2011	"Terminal functions" table has been corrected.
1.2	5-2011	Added Absolute Maximums Rating table Added packaging information
Rev 1.1	1-2011	Added RoHS compliancy Added revision history table