ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275

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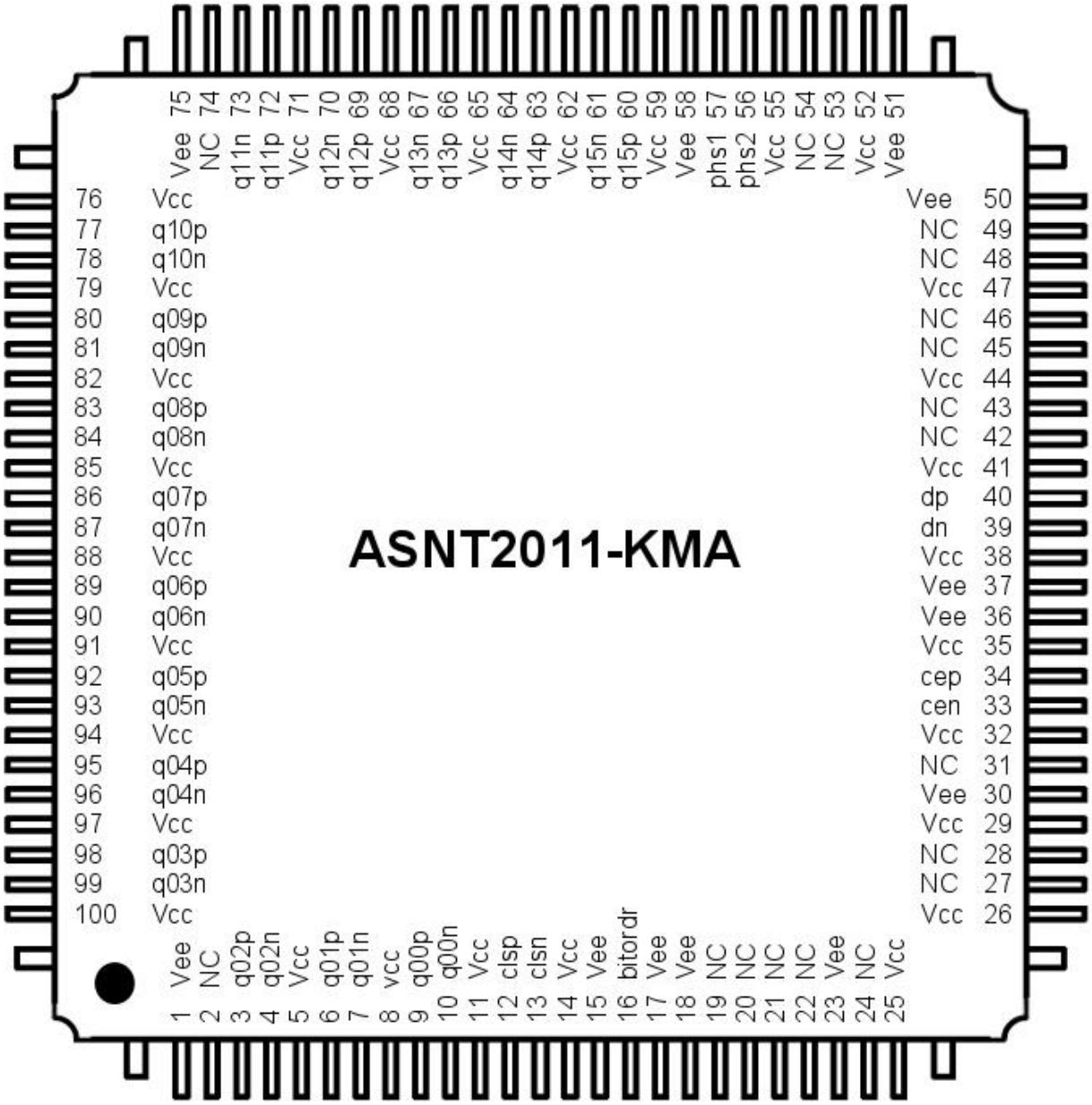
ASNT2011-KMA
DC-to-17*Gbps* Digital Demultiplexer 1:16 / Deserializer

- Broadband digital deserializer 1:16 operating seamlessly from DC to 17*Gbps*.
- LVDS output data buffers that feature a low-power proprietary architecture.
- Clock-divided-by-16 LVDS output buffer with 90°-step phase selection.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 730*mW* at 17*Gbps*.
- Custom 100-pin CQFP package (12*mm* x 12*mm*).



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DESCRIPTION

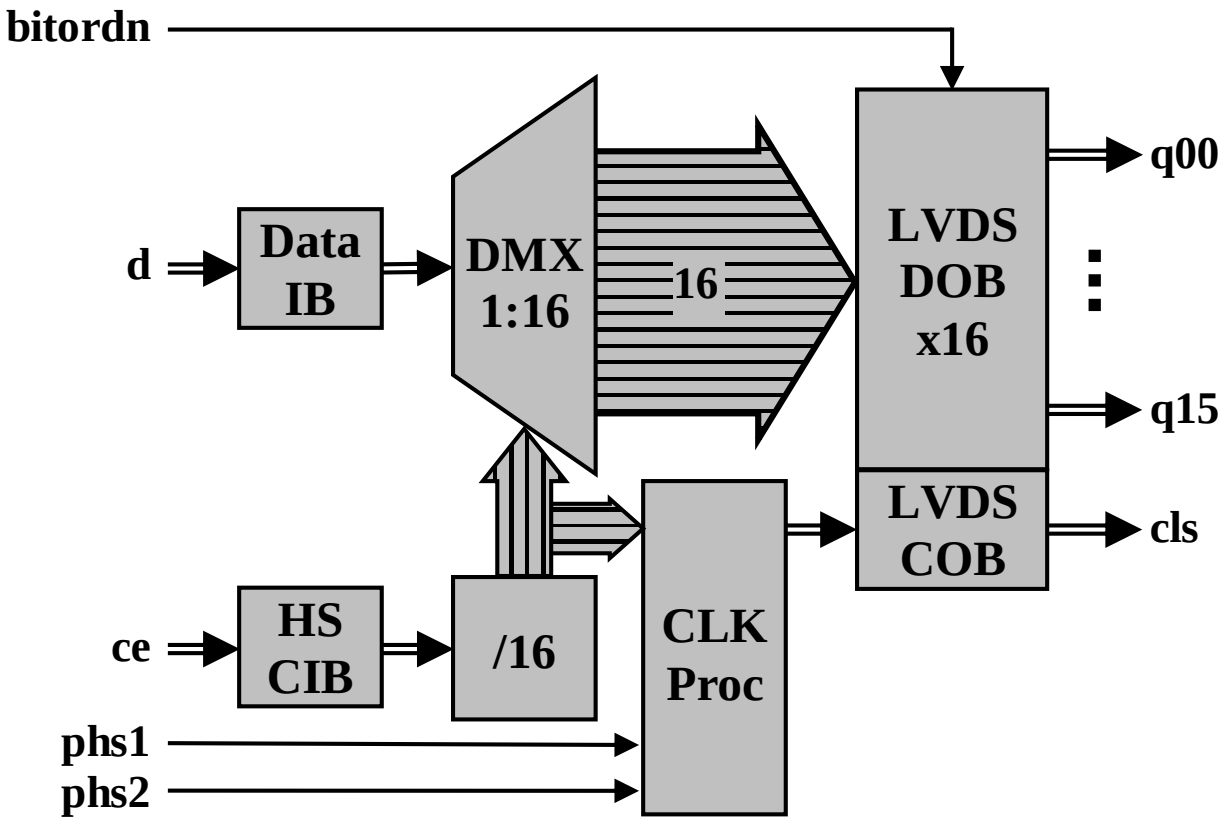

Fig. 1. Functional Block Diagram.

ASNT2011-KMA is a low power and high-speed digital 1 to 16 demultiplexer (DMUX) / deserializer IC. The IC shown in Fig. 1 can function seamlessly over input data rates (f_{bit}) ranging from DC to 17*Gbps*.

The main function of ASNT2011-KMA is to demultiplex a serial input data channel "d" running at a bit rate of f_{bit} into 16 parallel data channels "q00-q15" running at a bit rate of $f_{bit}/16$. The high sensitivity data input buffer (Data IB) ensures accurate operation for input data signal amplitudes greater than 40*mV* p-p differential or single-ended. It provides on-chip 50*Ohm* termination to "vcc" and is designed to be driven by devices with 50*Ohm* source impedance.

During normal operation, the received serial input data is latched into the tree-type demultiplexer (DMX1:16) and subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. The output MSB corresponds to "q00" when "bitordr"=0 (default), or to "q15" when "bitordr"=1.

A full rate clock must be provided by an external source "ce" to the high-speed clock input buffer (HS CIB) where it is routed to the internal divider-by-16 (/16). The divider provides signaling for DMX1:16 and produces a full rate clock divided-by-16 "C16" for the low speed LVDS compliant clock output buffer (LVDS COB). The phase of "cls" can be modified by 90° increments by utilizing pins "phs1" and "phs2" and the clock processing block (CLK Proc).

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Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals "q00-q15" while a similar LVDS clock output buffer (LVDS COB) outputs the low-speed clock signal "cls". The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards, while only consuming 30*mW* each.

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal "d" with bit rates from DC to 17*Gbps*. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. Data IB can handle input signal amplitudes between 40*mV* and 1.2*V* peak to peak (p-p) differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to "vcc" for each input line.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal "ce" with frequencies from DC to 17*GHz*. It can also accept a single-ended signal to one of its pins with a threshold voltage applied to the unused pin. HS CIB can handle input signal amplitudes between 200*mV* and 1.2*V* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to "vcc" for each input line.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock delivered by HS CIB is fed into the first divide-by-2 where its output is routed internally to the next divide-by-two circuit and outside of the block to DMX1:16. Other divided down clock signals are formed and routed to DMX1:16 in similar fashion. A full rate clock divided-by-16 "C16" is passed on to CLK Proc for additional phase adjustment.

DMX1:16

The 1 to 16 Demultiplexer (DMX1:16) utilizes a tree type architecture that latches in the data stream from Data IB on both edges of a half rate clock signal supplied by /16. The high speed data signal is subsequently demultiplexed down and delivered to LVDS DOBx16 in parallel fashion as 16-bit wide words running at a data rate up to 1063*Mbps*.

CLK Proc

By utilizing the CMOS control pins "phs1" and "phs2", the phase of "cls" can be altered in accordance with Table 1.

Table 1. Output Clock Phase Selection.

"phs1"	"phs2"	C16S phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

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LVDS DOBx16

The LVDS Data Output Buffer (LVDS DOBx16) accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards.

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives "C16" from CLK Proc and converts it into the LVDS output signal "cls". The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 standards. When "bitorder"=0 (default), "q00"is the MSB and when "bitorder"=1, "q15" is designated the MSB.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 2 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed "vee").

Table 2. Absolute Maximum Ratings.

Parameter	**Min**	**Max**	**Units**
Supply Voltage ("vee")		+3.6	*V*
Power Consumption		0.8	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	40	Input	CML differential data inputs with internal SE 50*Ohm* termination to "vcc".
dn	39		
cep	34	Input	CML differential clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	33		
Controls			
phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low).
phs2	56		

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bitordr	16	LS In., CMOS	Output bit order selection (active: high, q15 is MSB; default: low, q00 is MSB).

TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
q00n	10	Output	LVDS data outputs.
q00p	9		
q01n	7		
q01p	6		
q02n	4		
q02p	3		
q03n	99		
q03p	98		
q04n	96		
q04p	95		
q05n	93		
q05p	92		
q06n	90		
q06p	89		
q07n	87		
q07p	86		
q08n	84		
q08p	83		
q09n	81		
q09p	80		
q10n	78		
q10p	77		
q11n	73		
q11p	72		
q12n	70		
q12p	69		
q13n	67		
q13p	66		
q14n	64		
q14p	63		
q15n	61		
q15p	60		
clsp	12	Output	LVDS clock outputs. Can transmit four different clock phases as defined by “phs1” and “phs2”.
clsn	13		

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Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V*)	5, 8, 11, 14, 25, 26, 29, 32, 35, 38, 41, 44, 47, 52, 55, 59, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100.
vee	Negative power supply. (GND or 0*V*)	1, 15, 17, 18, 23, 30, 36, 37, 50, 51, 58, 75.
nc	Unconnected pin.	2, 19, 20, 21, 22, 24, 27, 28, 31, 42, 43, 45, 46, 48, 49, 53, 54, 74.

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
		General Parameters			
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	
Power consumption		730		*mW*	
Junction temperature	-25	50	125	*°C*	
		HS Input Data (d)			
Data Rate	0		17	*Gbps*	
Swing p-p (Diff or SE)	0.04		1.2	*V*	Peak-to-peak
CM Voltage Level	“vcc”-0.8		“vcc”	*V*	
		HS Input Clock (ce)			
Frequency	0.0		17	*GHz*	
Swing p-p (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	“vcc”-0.8		“vcc”	*V*	
Duty Cycle	40%	50%	60%		
		LS Output Data (q00-q15)			
Data Rate	0.0		1063	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		LS Output Clock (cls)			
Frequency	0.0		1063	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		CMOS Control Inputs/Outputs			
Logic “1” level	“vcc”-0.4			*V*	
Logic “0” level			“vee”+0.4	*V*	
		Timing Parameters			
“cls” to “q0-q15” delay variation		±2.5%			Over the full temperature range

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PACKAGE INFORMATION

The chip die is housed in a custom 100-pin CQFP package. The dimensioned drawings are shown in Fig. 2.

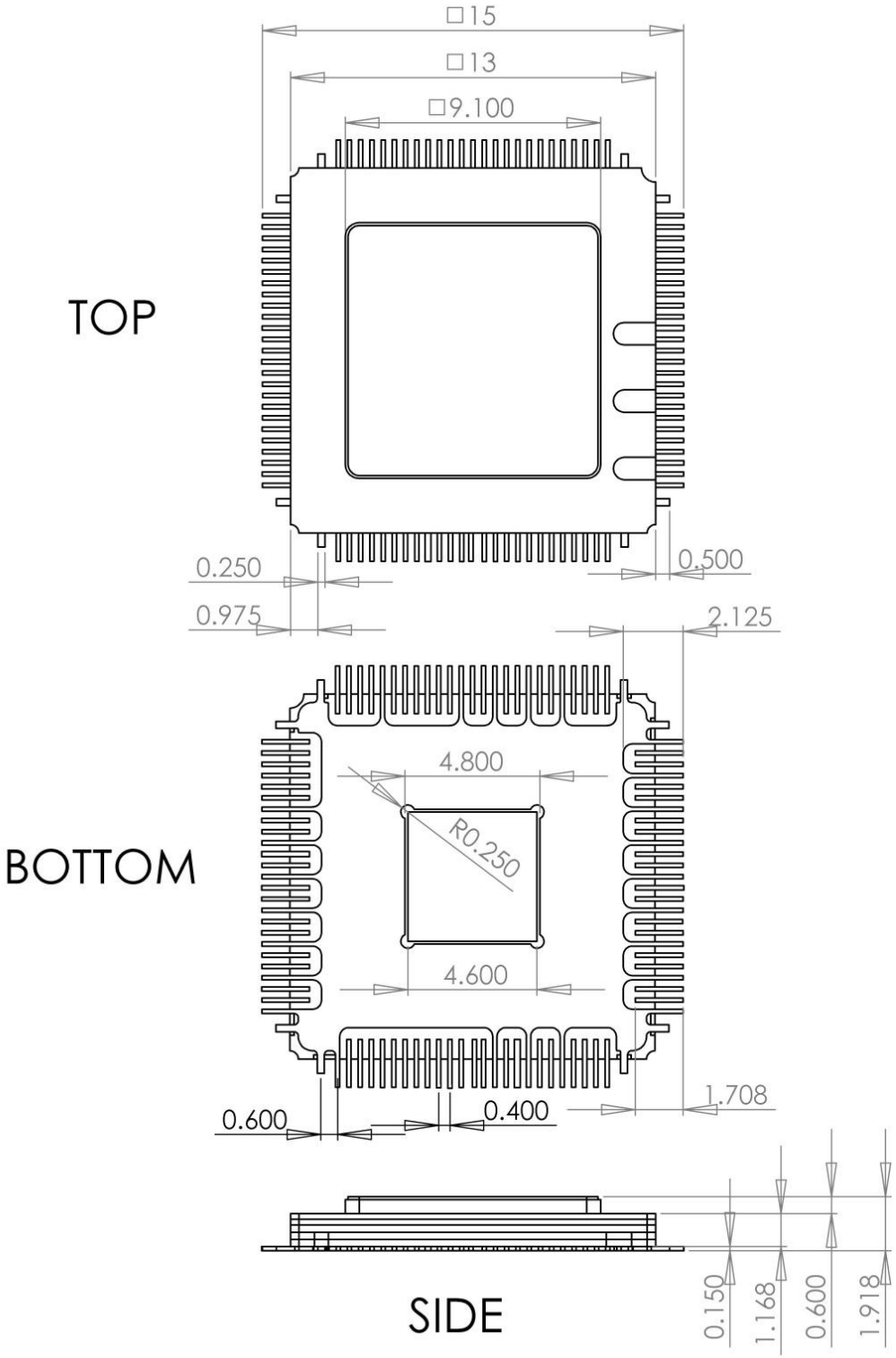

Fig. 2. Package Drawing.

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The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   3.9.1 Solderability
   3.2.2 Solder Purity Maintenance
   3.9.2 Solderability Maintenance
   3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder.

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the "vcc" plain, which is power for the positive supply.

The part's identification label is ASNT2011-KMA. The first 8 digits of the name before the underscore identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 digits after the underscore represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per EU 2002/95/EC for all six substances.

REVISION HISTORY

Revision	Date	Changes
3.1	2-2012	Revised Description section Revised Package Information section
3.0	1-2012	Added Absolute Maximums Rating table Revised Electrical Characteristics section Revised Package Information section
2.0	2-2009	Revised Electrical Characteristics section Revised Package Information section
1.0	1-2009	First release