ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Sience And Novel Technologies Company, Inc.
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ASNT2032-MBL
12:24 DMUX with LVDS Interface

- 12:24 digital demultiplexer (DMUX) with LVDS/CML/ECL input and output interfaces.
- Supports data rates from 1.0*Mbps* to 3.0*Gbps*.
- Preset function for synchronization of multiple parallel devices.
- Two pairs of clock divided-by-2 and synchronous clock enable outputs for supporting the tree-type demultiplexation structure.
- Synchronous clock divided-by-4 output may be chosen in place of clock divided-by-2 output.
- Power supply of +3.3*V*.
- Industrial temperature range.
- Low power consumption of 850*mW* at 3.0*Gbps*.
- Available in custom 256-pin BGA package (13*mm* x 13*mm* x 2.5*mm*).

DESCRIPTION

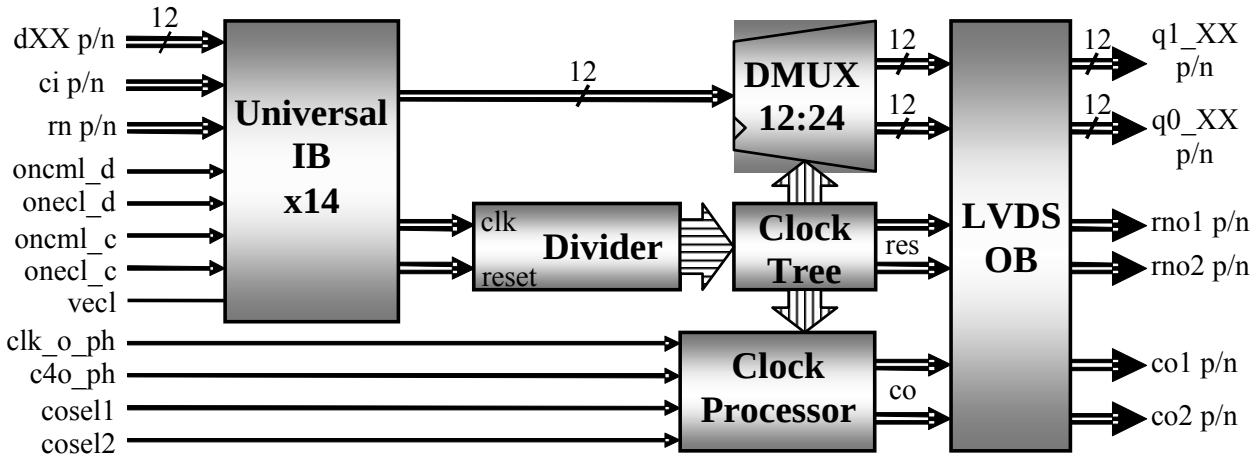


Fig. 1. Functional Block Diagram.

ASNT2032 is a broad-band 1*Mbps*-to-3*Gbps* multi-channel digital deserializer-demultiplexer (DMUX) 12-to-24 with external initial preset function and selectable LVDS, CML or ECL input and LVDS output interfaces. The part also features selectable clock divided-by-2 or clock divided-by-4 outputs with multiple phases. The latter is intended for DDR interface support.

The operational speed of DMUX is defined by an external clock signal ("ci p/n") that is converted into required timing signals by the internal divider. The divider can be preset to a certain initial state by an external active-low reset signal ("rn p/n"), which allows synchronization of multiple DMUX devices operating in parallel.

The optimal alignment of input data ("dXX p/n") and clock is illustrated in Fig. 2. The actual values of setup (t_{setup}) and hold (t_{hold}) times are presented in Table 6.

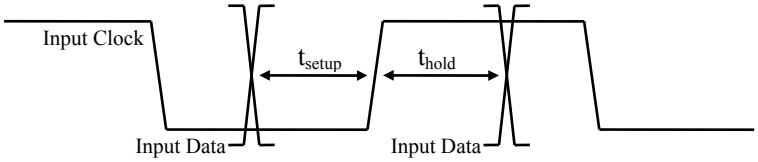


Fig. 2. Input Timing Diagram.

This part also supports cascaded tree-type structures as shown in Fig. 3, by supplying two synchronous copies of clock divided-by-2 ("co1 p/n" and "co2 p/n") and clock enable ("rno1 p/n", "rno2 p/n") signals.

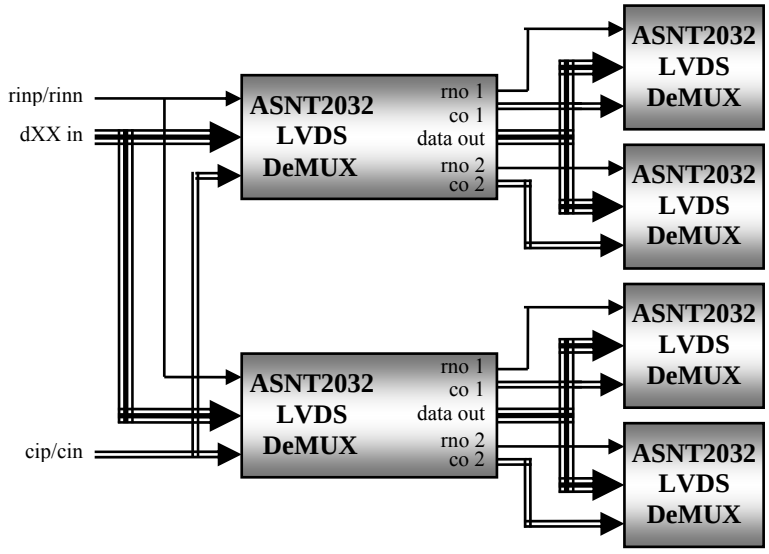


Fig. 3. Cascaded Tree-Type Structure.

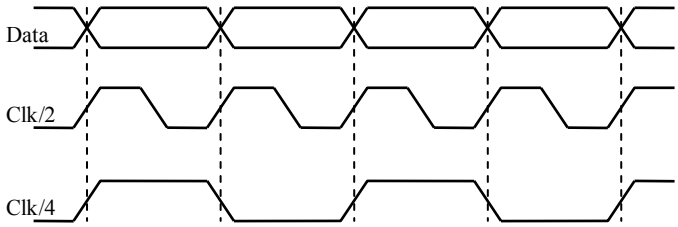
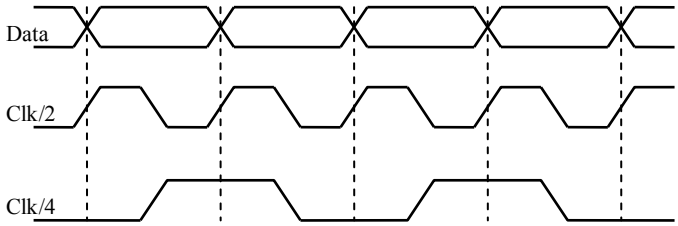
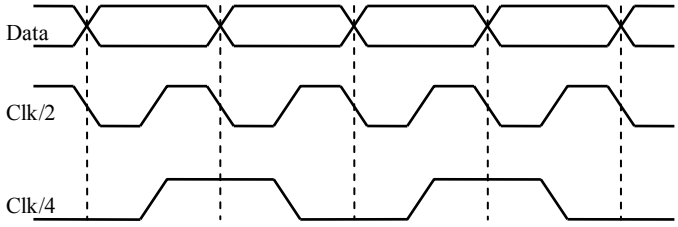
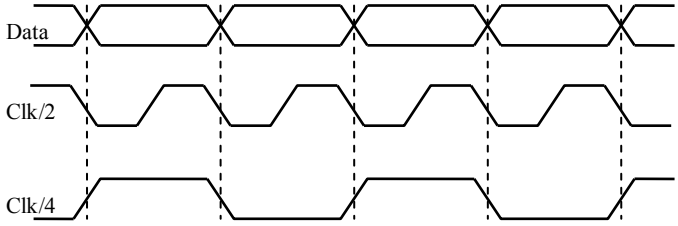
Clock divided-by-4 output signal can also be provided for higher flexibility instead of clock divided-by-2. Type of the output clock ("co1 p/n" and "co2 p/n") can be controlled by the "cosel1" and "cosel2" signals with values shown in Table 1.

Table 1. Clock divided-by-2 and clock divided-by-4 selection

cosel1 or cosel2 value	Clock output
0 (default)	Clk/2
1	Clk/4

All chip outputs are phase aligned with each other, with the capability to select the output clock phase relative to the output data. They are also stabilized over PVT variations. The shift is achieved by applying the "c4o_ph" and "clk_o_ph" signals. The defined phase relations are are shown in Table 2.

Table 2. Output clock phase selection

clk_o_ph	c4o_ph	
0	0	Clk/2 rising edges and Clk/4 edges are syncronous with data transition. 
	1	Only Clk/4 edges are shifted from data transition (half data period). 
1	0	Clk/2 rising edges and Clk/4 edges are shifted from data transition (half data period). 
	1	Only Clk/2 edges are shifted from data transition (half data period). 

The DMUX IC uses one power supply: "vcc"= +3.3*V* for the internal circuitry. It consumes about 850*mW* of power and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

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LVDS/ECL/CML Input Buffers

The input buffer for the data and divider reset signals may operate with LVDS, ECL or CML interfaces. The clock input buffer may only be used as CML or LVDS. To select the desired interface, refer to Table 3 .

Table 3. Input interface selection

on_ecl	on_cml	Interface
0 (default)	0 (default)	LVDS
1	0	ECL
0	1	CML
1	1	Not Allowed

When used in ECL mode, the "vecl" voltage must be set to 2*V* below "vcc".

DeMUX 12:24

The block consists of 12 independent demultiplexers 1-to-2 with the standard M-S/M-S-S architecture. It latches in the data signals on both edges of half-rate clock "c/2" that is supplied by the internal divider and delivers the deserialized outputs aligned to the corresponding clock edges. The output data signals are marked with "1" and "2" and are both aligned to the positive edge of the output clock divided-by-2.

Divider-by-4

The Divider-by-4 converts the input clock signal ("ci p/n") into clock divided-by-2 ("c/2") and clock divided-by-4 ("c/4") signals internally aligned to the positive edge of the input clock. The divider can be preset to the 0 initial state by external active-low "rn p/n" signal that is preliminarily retimed by the input clock.

LVDS Output Buffers

The LVDS output buffers are designed in full compliance with the LVDS standard and operate from a 3.3*V* supply at frequencies up to 3*GHz*. The output of the buffer must be 100*Ohm* differentially terminated.

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Terminal Functions

The ball assignment for the BGA package is shown in Table 4 and Table 5.

Table 4. Package Signal Balls.

Name	Code	Type	Description
High-Speed Inputs			
dp00	A8	LVDS, CML, or ECL	Differential data inputs
dn00	A7		
dp01	A6		
dn01	A5		
dp02	A4		
dn02	A3		
dp03	A2		
dn03	A1		
dp04	B1		
dn04	C1		
dp05	D1		
dn05	E1		
dp06	M1		
dn06	N1		
dp07	P1		
dn07	R1		
dp08	T1		
dn08	T2		
dp09	T3		
dn09	T4		
dp10	T5		
dn10	T6		
dp11	T7		
dn11	T8		
rnp	J1		Differential divider reset input
rnn	K1		
cip	G1	LVDS or CML	Differential clock inputs
cin	H1		
High-Speed Outputs			
rno1p	A9		Differential divider reset outputs
rno1n	B9		
rno2p	T9		
rno2n	R9		
co1p	H16		Differential clock outputs
co1n	H15		
co2n	J16		
co2p	J15		

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Name	Code	Type	Description
q0p<00>	B10	LVDS output	Differential data outputs
q0n<00>	A10		
q1p<00>	B11		
q1n<00>	A11		
q0p<01>	B12		
q0n<01>	A12		
q1p<01>	B13		
q1n<01>	B14		
q0p<02>	A13		
q0n<02>	A15		
q1p<02>	A14		
q1n<02>	A16		
q0p<03>	B15		
q0n<03>	B16		
q1p<03>	C15		
q1n<03>	C16		
q0p<04>	D15		
q0n<04>	D16		
q1p<04>	E15		
q1n<04>	E16		
q0p<05>	F15		
q0n<05>	F16		
q1p<05>	G15		
q1n<05>	G16		
q0p<06>	K15		
q0n<06>	K16		
q1p<06>	L15		
q1n<06>	L16		
q0p<07>	M15		
q0n<07>	M16		
q1p<07>	N15		
q1n<07>	N16		
q0p<08>	R16		
q0n<08>	P16		
q1p<08>	T16		
q1n<08>	P15		
q0p<09>	T14		
q0n<09>	R15		
q1p<09>	T13		
q1n<09>	T15		
q0p<10>	R13		
q0n<10>	R14		

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Name	Code	Type	Description
q1p<10>	R12	LVDS output	Differential data outputs
q1n<10>	T12		
q0p<11>	R11		
q0n<11>	T11		
q1p<11>	R10		
q1n<11>	T10		
Low-Speed Control Signals			
cosel1	M8	3.3V CMOS DC	CMOS control signals
cosel2	N8		
clk_o_ph	P8		
c4o_ph	P7		
oncml_c	D6, N6		
onecl_d	D9		
oncml_d	D8		

Table 5. Package Power Supply Balls.

Name	Code	Type	Value, *V*
vee	B2-B8, C2-C14, D2-D4, D10-D14, E2-E14, F2-F4, F12-F14, G2-G4, G12-G14, H2-H4, H12-H14, J2-J4, J12-J14, K2-K4, K12-K14, L2-L4, L12-L14, M2-M7, M10-M14, N2-N5, N9-N14, P2-P6, P9-P14, R2-R8	Ground	0
vcc	F7-F11, G6, G7, G9-G11, H10, J10, K6, K7, K9-K11, L7, L9-L11, M9	Positive supply voltage	3.3
vecl	F6, G8, H5, H6, H7, J5, J6, J7, K8, L6, L8	ECL input termination voltage	vcc-2*V*
n/c	F1, L1	Not connected	
X	D5, D7, F5, G5, H8, H9, H11, J8, J9, J11, K5, L5, N7	Removed balls	

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ELECTRICAL CHARACTERISTICS

Table 6. Electrical characteristics

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
Power consumption		850		*mW*	
Junction temperature	-25	50	125	*°C*	
Input Data (dXX p/n)					
Data Rate	1		3000	*Mbps*	
Swing (SE)	50		600	*mV*	Peak-to-peak
CM Voltage Level	1		3.3	*V*	
Interface					LVDS, ECL, CML
Input Clock (ci p/n)					
Frequency	1		3000	*MHz*	
Swing (SE)	50		600	*mV*	Peak-to-peak
CM Voltage Level	1		3.3	*V*	
Interface					LVDS, CML
Output Data (q0_XX, q1_XX)					
Data Rate	0.5		1500	*Mbps*	
Swing (SE)	250	325	400	*mV*	Peak-to-peak
CM Voltage Level	1.125	1.2	1.275	*V*	
Interface		LVDS			
Divided Output Clock (co1 p/n, co2 p/n)					
Frequency	0.5/0.25		1500/750	*MHz*	
Swing (SE)	250	325	400	*mV*	Peak-to-peak
CM Voltage Level	1.125	1.2	1.275	*V*	
Interface		LVDS			
Timing Parameters					
Data skew		0		*ps*	By simulation
Clock skew		0		*ps*	
τ_{setup}		-90		*ps*	
τ_{hold}		200		*ps*	

PACKAGE INFORMATION

The chip is packaged in a custom 256-pin BGA package.