ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Sience And Novel Technologies Company, Inc.
27 Via Porto Grande, Rancho Palos Verdes, CA 90275
Phone: **310-377-6029 / 310-803-9284 | *Fax:* 310-377-9940**
Website: **www.adsantec.com**

ASNT2031-MBL
24:48 DMUX with SSTL Interface

- 24:48 digital demultiplexer (DMUX) with SSTL1.5 input and output interfaces.
- Supports data rates from 1.0*Mbps* to 2.0*Gbps*.
- User-controllable independent internal delays for data and clock signals.
- 3.0*V* I^2C control interface with a user-defined 3-bit chip address.
- Preset function for synchronization of multiple parallel devices.
- Full-rate output copy of external high-speed clock input signal.
- Two pairs of clock divided-by-2 and synchronous clock enable outputs for supporting the tree-type demultiplexation structure.
- Additional synchronous clock divided-by-4 output.
- Dual power supply of +3.0*V* and +1.5*V*.
- Industrial temperature range.
- Low power consumption of 2.1*W* at 2.0*Gbps*.
- Available in custom 256-pin BGA package (13*mm* x 13*mm* x 2.5*mm*).

DESCRIPTION

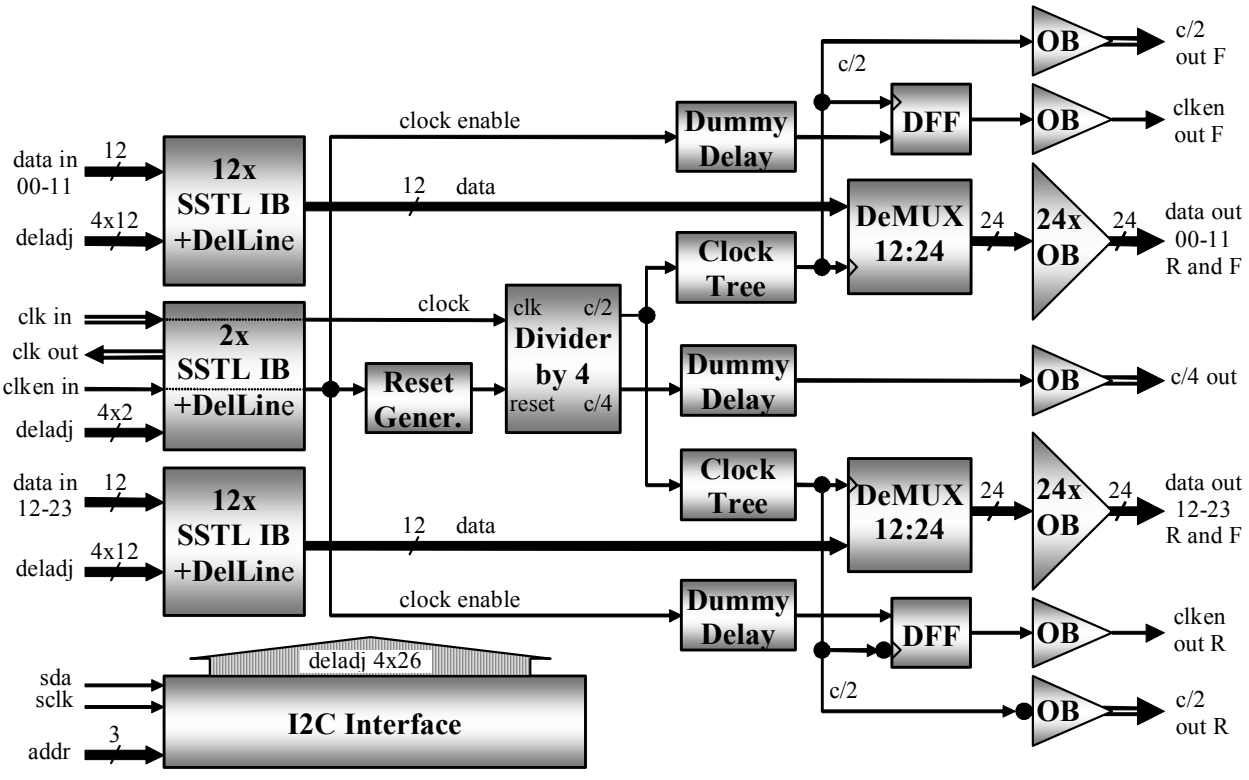

Fig. 1. Functional Block Diagram.

ASNT2031-MBL is a broad-band 1.0*Mbps*-to-2.0*Gbps* multi-channel digital deserializer-demultiplexer (DMUX) 24-to-48 with external initial preset functionality and 1.5*V* single-ended SSTL1.5 input and output interfaces for data and preset signals, as well as matching differential interfaces for clock signals.

The part includes active variable delay lines (DelLine) in each input data and clock path for accurate signal alignment at the DMUX register inputs in order to define the optimal sampling point for the input data signals ("data in"). The value of each delay is externally controlled through an I^2C interface with a user-selectable 3-bit chip address.

The operational speed of DMUX is defined by an external clock signal ("clk in") that is converted into the required timing signals by an internal divider and is also supplied to the output of the chip ("clk out"). The divider can be preset to a certain initial state by the external clock enable signal ("clken in"), which allows synchronization of multiple DMUX devices operating in parallel.

The optimal alignment of input data ("data in") and clock is illustrated in Fig. 2. The actual values of setup (t_{SU}) and hold (t_H) times are presented in Table 5.

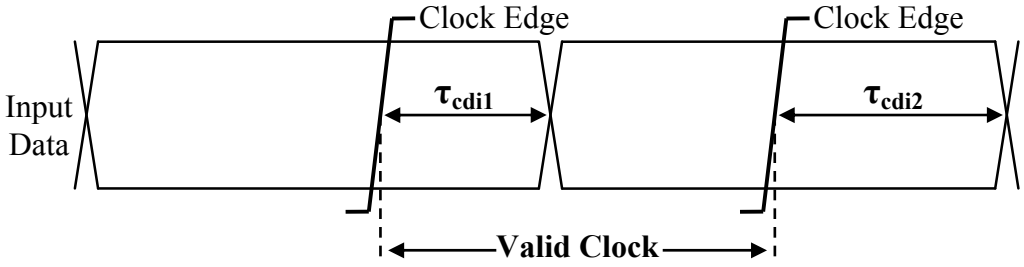

Fig. 2. Input Timing Diagram.

This part also supports cascaded tree-type structures as shown in Fig. 3, by supplying two synchronous copies of clock divided-by-2 ("c/2 F", "c/2 R") and clock enable ("clken F", "clken R") signals.

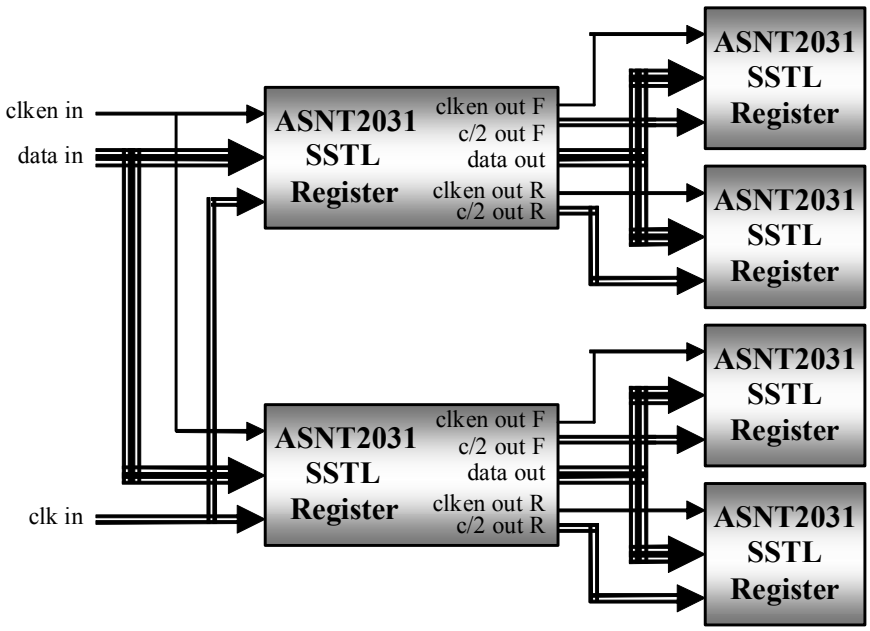

Fig. 3. Cascaded Tree-Type Structure.

Clock divided-by-4 ("c/4 out") output signal is also provided for higher flexibility.

All clock and clock enable outputs are phase-aligned as shown in Fig. 4. The defined phase relations are stabilized over PVT variations.

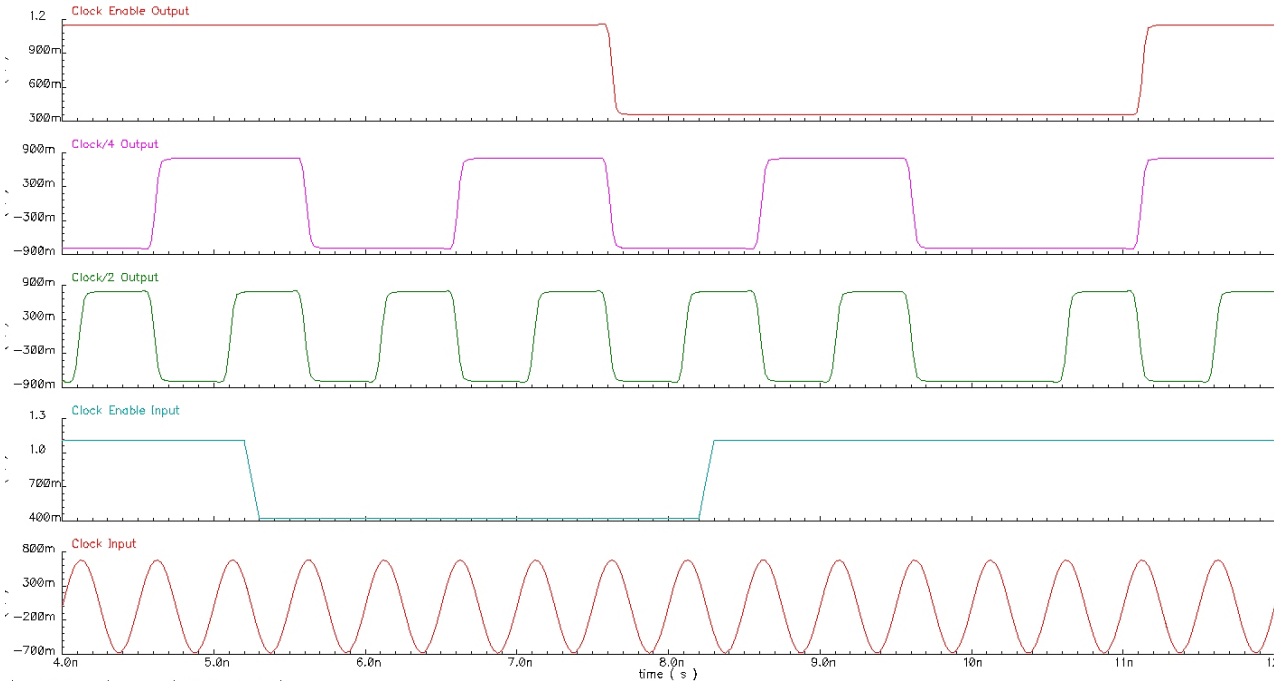

Fig. 4. Clock Signals.

The output data alignment to the output clock divided-by-2 is illustrated in Fig. 5. This relation is also stabilized over PVT variations. The actual values of setup (t_{SU}) and hold (t_H) times are presented in Table 5.

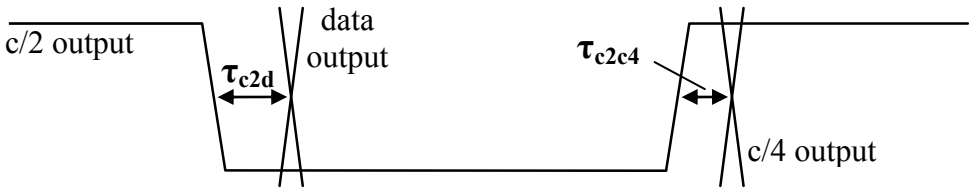

Fig. 5. Output Data Alignment.

The DMUX IC uses two power supplies: "vdd"= +1.5*V* for CMOS I/Os and "vcc"= +3.0*V* for the internal circuitry. It consumes about 2.1*W* of power and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

SSTL Input Buffers

The SSTL input buffer is designed as a differential current switch with high tolerance to input common-mode voltage level variation. In a differential mode used for clock inputs, it accepts two complementary signals and provides a selectable internal termination for both of them depending on the state of an internal switch. The switch is controlled by external 3.0*V* CMOS

signal "term on" as shown in Table 1. A special external voltage "vtt"="vdd"/2 should be provided for the correct operation of the termination circuit.

Table 1. Input Termination States.

"term_on" signal state	Switch state	Termination type
High	Closed	50Ohm to "vtt"
Low	Open	High impedance

The buffer can also operate in a single-ended mode used for data and clock enable inputs. In this mode, it accepts one input signal and external reference voltage "vref"="vdd"/2. Deviations of the reference voltage may result in the duty cycle distortion of input signals.

Delay Lines

Digitally-controlled on-chip active delay lines are used for the alignment of input clock and data signals in order to achieve the optimal sampling conditions at the inputs of the demultiplexer's internal register. Each delay line has 15 states with an absolute delay from 400*ps* to 1400*ps*. The accuracy of the minimum delay value is within ±20% for the full PVT range. This relatively high variation is insignificant for the chip operation due to the matching delays in all input paths. The additional controllable delay of 1*ns* is highly stabilized and falls within ±5% accuracy range.

The states of the delay lines are controlled within the 1-2-4-8 algorithm by signals provided from the internal I^2C interface.

DeMUX 24:48

The block consists of 24 independent demultiplexers 1-to-2 with the standard M-S/M-S-S architecture. It latches in the data signals on both edges of half-rate clock "c/2" that is supplied by the internal divider-by-4 and delivers the deserialized outputs aligned to the corresponding clock edges. The output data signals are marked "A" and "B" and are aligned to the rising edge of "c/2".

Divider-by-4

The Divider-by-4 converts the input clock signal ("clk in") into clock divided-by-2 ("c/2") and clock divided-by-4 ("c/4") signals aligned to a positive edge of the input clock. The divider can be preset to the 0 initial state by the external "clken in" signal that is preliminarily retimed by the input clock.

SSTL Output Buffers

The SSTL output buffers are designed in full compliance with the SSTL1.5 standard and operate from a nominal 1.5*V* supply. Their CMOS driver can source or sink the required current through a 25*Ohm* series resistor. The output of the buffer may be 50*Ohm* terminated to an external voltage equal to a half of the buffer's supply voltage, or left non-terminated.

Clock Enable and Divider Reset

The clock enable signal must be at least 2 high-speed input clock periods long. The clock enable signal must be aligned with the falling edge of the high-speed input clock.

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I²C Interface

This 2-wire 3.0*V* serial-to-parallel interface with initial preset (with an all "0" address word for reset) is used for setting the values of internal delays in the data and clock paths. The chip incorporates a Slave I²C device that supports write operations as described below.

The I²C system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. Data is transferred between Master and Slave synchronously on a byte-by-byte basis. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledgement bit set by Slave follows each transferred byte. Each bit is sampled during the high period of SCL.

The first byte of data transferred by Master immediately after START signal is the requested slave address. It consists of Vendor/Device code (currently 0xD) followed by Chip Address "Addr[2:0]" and an RW bit. The address of DMUX chip is defined by hard-wiring of 3 corresponding pins to either "vee" or "vcc". The RW bit defines the type of operation: writing information from Master to Slave, or reading information by Master from Slave.

When RW=0 (write operation) and the requested address matches the preset slave address, the chip's I²C block responds by pulling the following bit (9-th acknowledgement bit) low. It then saves 4 LSBs of the next byte in the Input Address Register and returns another acknowledgement bit at the end of the second byte. After that, the block saves the next byte in the Input Data Register and returns acknowledgement bit one more time. During the same time, the interface transfers the previously stored byte of data from the Input Data Register to the internal register in accordance with the 4-bit address previously saved in the Input Address Register. The address assignment is detailed in Table 2.

Table 2. Internal Address Assignments.

Address	Destination	Data
1'b0000	Not Used	
1'b0001	Delay for Data Channel 13 and 1	Data[7:4] and Data[3:0]
1'b0010	Delay for Data Channel 14 and 2	Data[7:4] and Data[3:0]
1'b0011	Delay for Data Channel 15 and 3	Data[7:4] and Data[3:0]
1'b0100	Delay for Data Channel 16 and 4	Data[7:4] and Data[3:0]
1'b0101	Delay for Data Channel 17 and 5	Data[7:4] and Data[3:0]
1'b0110	Delay for Data Channel 18 and 6	Data[7:4] and Data[3:0]
1'b0111	Delay for Data Channel 19 and 7	Data[7:4] and Data[3:0]
1'b1000	Delay for Data Channel 20 and 8	Data[7:4] and Data[3:0]
1'b1001	Delay for Data Channel 21 and 9	Data[7:4] and Data[3:0]
1'b1010	Delay for Data Channel 22 and 10	Data[7:4] and Data[3:0]
1'b1011	Delay for Data Channel 23 and 11	Data[7:4] and Data[3:0]
1'b1100	Delay for Data Channel 24 and 12	Data[7:4] and Data[3:0]
1'b1101	Delay for Clock Enable and Clock	Data[7:4] and Data[3:0]
1'b1110	Not Used	
1'b1111	Delay for Data Channels 13-to-24 and 1-to-12	Data[7:4] and Data[3:0]

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Terminal Functions

The ball assignment for the BGA package is shown in Table 3 and Table 4.

Table 3. Package Signal Balls.

Name	Code	Type	Description
High-Speed Inputs			
data in 00	A8	1.5*V* CMOS input	Single-ended data inputs
data in 01	A7		
data in 02	A6		
data in 03	A5		
data in 04	A4		
data in 05	A3		
data in 06	A2		
data in 07	A1		
data in 08	B1		
data in 09	C1		
data in 10	D1		
data in 11	E1		
data in 12	M1		
data in 13	N1		
data in 14	P1		
data in 15	R1		
data in 16	T1		
data in 17	T2		
data in 18	T3		
data in 19	T4		
data in 20	T5		
data in 21	T6		
data in 22	T7		
data in 23	T8		
clk in p	G1		Differential clock inputs
clk in n	H1		
clken in	F1		Single-ended clock enable input
High-Speed Outputs			
clk out p	J1	SSTL 1.5*V* output	Differential clock outputs
clk out n	K1		
c/2 out A p	T9		Differential clock outputs
c/2 out A n	R9		
c/2 out B p	A9		Differential clock outputs
c/2 out B n	B9		
c/4 out p	H16		Differential clock outputs
c/4 out n	H15		
clken out A	J16		Single-ended clock enable output
clken out B	J15		Single-ended clock enable output

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Name	Code	Type	Description
data out A 00	B10	SSTL 1.5*V* output	Single-ended data outputs
data out B 00	A10		
data out A 01	B11		
data out B 01	A11		
data out A 02	B12		
data out B 02	A12		
data out A 03	B13		
data out B 03	B14		
data out A 04	A13		
data out B 04	A15		
data out A 05	A14		
data out B 05	A16		
data out A 06	B15		
data out B 06	B16		
data out A 07	C15		
data out B 07	C16		
data out A 08	D15		
data out B 08	D16		
data out A 09	E15		
data out B 09	E16		
data out A 10	F15		
data out B 10	F16		
data out A 11	G15		
data out B 11	G16		
data out A 12	K15		
data out B 12	K16		
data out A 13	L15		
data out B 13	L16		
data out A 14	M15		
data out B 14	M16		
data out A 15	N15		
data out B 15	N16		
data out A 16	R16		
data out B 16	P16		
data out A 17	T16		
data out B 17	P15		
data out A 18	T14		
data out B 18	R15		
data out A 19	T13		
data out B 19	T15		
data out A 20	R13		
data out B 20	R14		

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Name	Code	Type	Description
data out A 21	R12	SSTL 1.5*V* output	Single-ended data outputs
data out B 21	T12		
data out A 22	R11		
data out B 22	T11		
data out A 23	R10		
data out B 23	T10		
sda	M9	SSTL 1.5*V* input	Single-ended control inputs
sclk	M8		
add1	N8	3*V* DC CMOS	Delay control word
add2	P8		
add3	P7		
dton	D9	3*V* DC CMOS	"term on" for data
cton	D8		"term on" for clock, clk_en

Table 4. Package Power Supply Balls.

Name	Code	Type	Value, *V*
vee	B2-B8, C2-C14, D2-D4, D10-D14, E2-E14, F2-F4, F12-F14, G2-G4, G12-G14, H2-H4, H12-H14, J2-J4, J12-J14, K2-K4, K12-K14, L2-L4, L12-L14, M2-M7, M10-M14, N2-N5, N9-N14, P2-P6, P9-P14, R2-R8	Ground	0
vcc	F8, F9, F10, G9, K9, L9, L10	Analog positive supply voltage	3.0
vdd	F7, F11, G6, G7, G10, G11, H10, J10, K6, K7, K10, K11, L7, L11	Digital positive supply voltage	1.5
vtt	F6, G8, H5, H6, H7, J5, J6, J7, K8, L6, L8	SSTL input termination voltage	vdd/2
vref	D6, N6	Reference voltage for SSTL input buffers	vdd/2
n/c	D5, D7, F5, G5, H8, H9, H11, J8, J9, J11, K5, L1, L5, N7	Removed balls, Not connected	

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ELECTRICAL CHARCTERISTICS

Table 5. Electrical Characteristics.

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{DD}	+1.43	+1.5	+1.57		
V_{EE}		0.0		*V*	
Power consumption		2.1		*W*	
Junction temperature	-25	50	125	*°C*	
Input Data (data in)					
Data Rate	1		2000	*Mbps*	
Swing (SE)		1.5		*V*	Peak-to-peak
CM Voltage Level		750		*mV*	
Allowed V_{IH} range	1.1		1.8	*V*	
Allowed V_{IL} range	0		450	*mV*	
Input Clock (clk in)					
Frequency	1		2000	*MHz*	
Swing (SE)		1.5		*V*	Peak-to-peak
CM Voltage Level		750		*mV*	
Output Data (data out)					
Data Rate	0.5		1000	*Mbps*	
Swing (SE)		1.5		*V*	Peak-to-peak
CM Voltage Level		750		*mV*	
Interface		SSTL1.5			
HS Output Clock (clk out)					
Frequency	1		2000	*MHz*	
Swing (SE)		1.5		*V*	Peak-to-peak
CM Voltage Level		750		*mV*	
Interface		SSTL1.5			
Timing Parameters					
clk_in to clk_out	420	510	560	*ps*	Propagation delay
clk_in to c2_out	640	780	880	*ps*	
clk_in to c4_out	640	760	890	*ps*	
Data skew		0		*ps*	By simulation
Clock skew		0		*ps*	
τ_{cdi1}	200	245	300	*ps*	
τ_{cdi2}	230	275	330	*ps*	
τ_{c2d}	9	20	24	*ps*	
τ_{c2c4}	0	1	-1	*ps*	

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PACKAGE INFORMATION

The chip is packaged in a custom 256-pin BGA package. The drawing of the package is shown below.

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