ADSANTEC
Ultra High-Speed Mixed Signal ASICs
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ASNT2017-PQA
1:16 CDR-DMUX

- 1:16 demultiplexer (DMUX) with integrated full rate CDR (clock and data recovery).
- Supports data rates from 13.5*Gb/s* to 14.5*Gb/s* in the CDR mode.
- Supports data rates from DCto 15*Gb/s* in the optional digital mode.
- Proprietary low-power LVDS output data buffers.
- LVDS output clock-divided-by-16 with a selectable phase.
- Supports divided by 16 or by 64 input reference clocks in the CDR mode.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 890*mW* at 14*Gbps*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

DESCRIPTION

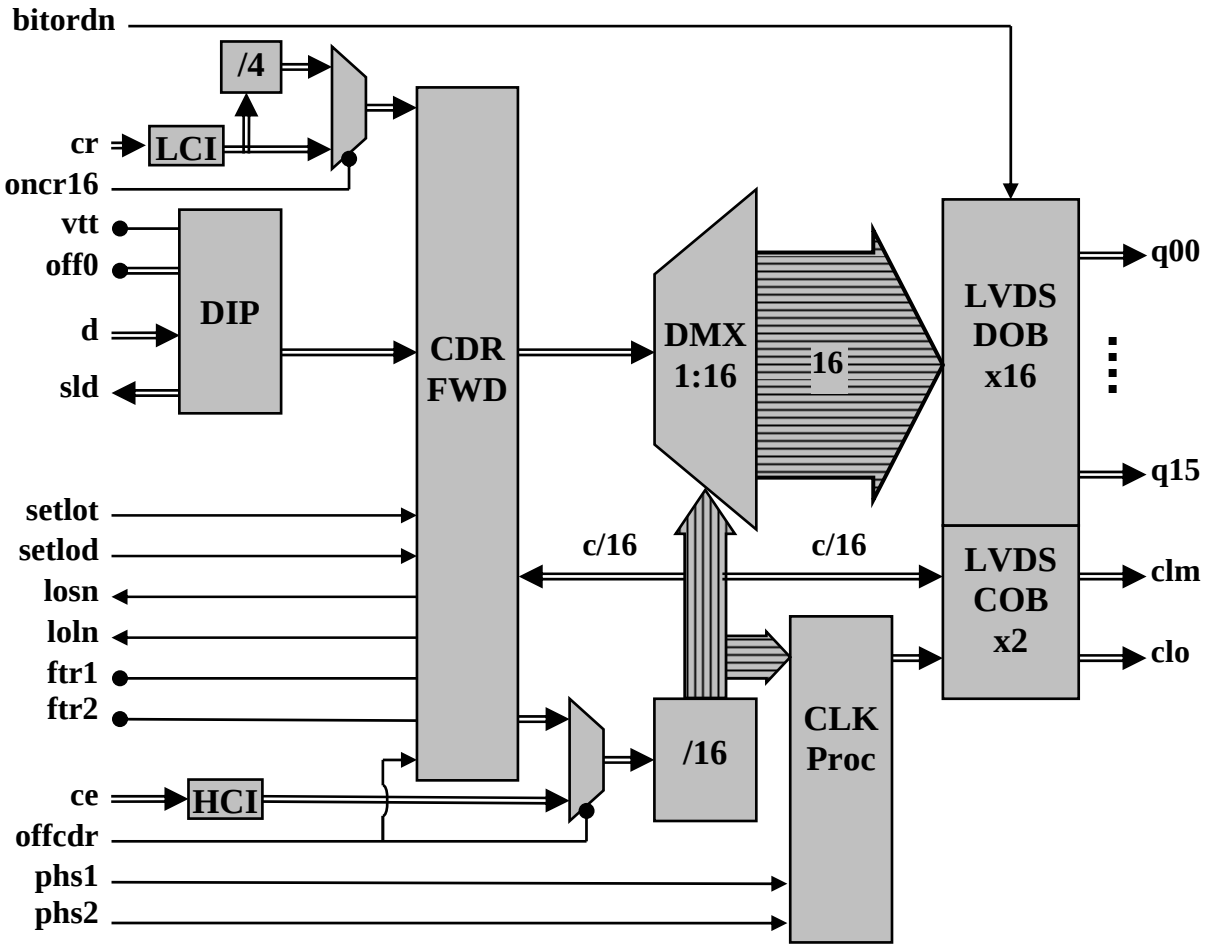

Fig. 1. Functional Block Diagram.

ASNT2017 is a user-programmable 14*Gbps* 1:16 deserializer (DMUX) with a full-rate integrated clock and data recovery unit (CDR) that incorporates a frequency window detector (FWD). The

main function of the chip is to demultiplex a serial input data channel "d" running at a bit rate of f_{bit} into 16 parallel data channels "q00-q15" running at a bit rate of $f_{bit}/16$. The DMUX can operate in one of two main modes: CDR mode that utilizes on-chip full-rate VCO with a central frequency of f_{bit} or broadband digital mode that requires application of an external full-rate clock "ce" with the same frequency to the inputs of a high speed CML clock input buffer (HS CIB). Selection of the operational mode is made through pin "offcdr".

The high sensitivity CDR FWD block incorporates phase and frequency acquisition loops to ensure accurate recovery of clock and data for NRZ input data stream. For the correct operation of the block, off-chip passive filter components should be connected to pins "ftr1" and "ftr2". CDR FWD als requires an external reference clock running at 1/16 or 1/64 the VCO's central frequency to be applied to input "cr". The acceptable frequency of the reference clock is defined by "oncr16" control signal. If the 1/16 mode is selected, the input clock is applied to CDR FWD after additional divider by 4 (/4). The reference clock input buffer supports LVDS or CML interfaces as defined by "oncml" control signal. The recovered clock is used to samples the input data bits before they are demultiplexed and is also sent to the internal divider (/16).

CDR FWD provides active-low alarm indicators for the loss of input signal ("losn") and loss of lock ("loln").

The high-speed CML data and clock input buffers provide on-chip 50*Ohm* termination and are designed to be driven by devices with 50*Ohm* source impedance. The data input buffer sets its termination voltage internally, but "vtt" pin can be used to externally adjust it if desired. Pins "off0" control the offset voltage between data inputs "dp" and "dn" allowing the user to change the slicing or threshold level at the serial data input. A peak detector is incorporated in Data IB to monitor the amplitude of the incoming data stream with its output made available through the differential pins "sld".

The reconstructed serial input data is latched into the demultiplexer (DMX1:16) and is subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. Utilizing pin "bitordn", the deserializer can designate either "q00" or "q15" as the MSB thus simplifying the interface between the demultiplexer chip and the following ASIC.

Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals "q00-q15" while a similar dual LVDS clock output buffer (LVDS COBx2) outputs the two copies of a low-speed clock signal ("clm" and "clo"). The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. The phase of "clo" clock signal can be selected with a 90° increment by utilizing pins "phs1" and "phs2".

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

Data IP

The Data Input Processor (Data IP) can process differential or single-ended CML signals with bit rates up to 15*Gbps*. The data inputs utilize on-chip single-ended 50*Ohm* termination to "vtt"=2.5*V* (default) for each input line where "vtt" can be also adjusted externally. A single-

ended data can be applied to one of the differential input pins either directly (DC coupling) or through a capacitor (AC coupling). In case of DC coupling, a threshold voltage must be set on the other pin. In case of AC coupling, the unused input pin must be terminated to "vtt". In any case, the duty cycle of the received signal can be adjusted using control inputs "off0n" or "off0p" with impedances of 250*Ohm*.

Additionally, Data IP includes an input signal peak detector that delivers its response through the output differential signal "sld". The detector can demodulate AM component(s) carried by the input data stream that are in the frequency range of up to a few hundred *kHz*. Each single-ended output of the peak detector has a 3.1*KOhm* impedance in relation to "vcc".

LCI

The Low-speed clock input buffer (LCI) consists of a proprietary universal input buffer that is designed to accept differential or single-ended signals as defined by external CMOS control signal "oncml". In the differential mode ("oncml"="0"), the input pins have internal differential termination of 100*Ohm* that is suitable for LVDS interface. The buffer can accept differential signals with DC common mode voltage variation from 0 to "vcc" and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. In the single-ended mode ("oncml"="1"), each input pin has a 50*Ohm* termination to "vcc". A single-ended clock can be applied to one of the differential input pins either directly (DC coupling) or through a capacitor (AC coupling). In case of DC coupling, a threshold voltage must be set on the other pin. In case of AC coupling, the unused input pin must be terminated to "vcc".

/4

The divider by 4 (/4) is used to adjust the external reference clock "cr" if its frequency is selected to be equal to 1/16 of the VCO's central frequency. The divider is activated by "oncr16" control signal and delivers a standard divided-by-64 reference clock to CDR FWD.

HCI

The high-speed clock input buffer (HCI) can accept external CML clock signals and provides on-chip single-ended termination of 50*Ohm* to "vcc" for each input line "cep" or "cen". A single-ended clock can be applied to one of the differential input pins either directly (DC coupling) or through a capacitor (AC coupling). In case of DC coupling, a threshold voltage must be set on the other pin. In case of AC coupling, the unused input pin must be terminated to "vcc".

CDR FWD

The clock and data recovery block with a frequency window detector (CDR FWD) contains both phase and frequency acquisition loops. The phase-locked loop requires an off-chip filter featuring a 1*nF* capacitor across the pins "ftr1" and "ftr2".

The main function of CDR FWD is to lock the frequency of the on-chip VCO to that of the input data signal (clock recovery) while adgusting the VCO's clock phase to latch in the incoming data with minimal error (data recovery). The recovered clock is also utilized by the internal divider (/16) to generate all internal timing signals.

CDR FWD raises the loss of signal "losn" flag when the input data's transition density is not enough or too much. A loss of lock "loln" is generated by CDR FWD when the frequency difference between the reference clock (corresponding to 1/64 of the VCO frequency) and internal clock divided-by-64 exceeds ±1000*ppm*.

/16

The divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock delivered by CDR FWD is fed into the first divide-by-2 where its output is routed internally to the next divide-by-two circuit and outside of the block to DMX1:16 through a buffering circuit. Other divided down clock signals are also buffered and routed to DMX1:16 in similar fashion. The clock divided-by-16 "c/16" is passed on to one LVDS OB and to CLK Proc for additional phase adjustment.

DMX1:16

The 1 to 16 demultiplexer (DMX1:16) utilizes a tree type architecture and latches in the data stream from CDR FWD on both edges of a half-rate clock signal that is supplied by the divider (/16). The high speed data signal is subsequently demultiplexed down and delivered to LVDS data output buffers (LVDS DOBx16) as16-bit wide parallel words.

CLK Proc

By utilizing the CMOS control pins "phs1" and "phs2", the phase of the main low-speed clock output signal ("clo") can be selected in accordance with the table below.

Table 1. Clock Phase Selection.

"phs1"	"phs2"	"clo" phase
V_{EE} (default)	V_{EE} (default)	270°
V_{EE}	V_{CC}	180°
V_{CC}	V_{EE}	90°
V_{CC}	V_{CC}	0°

LVDS DOBx16

LVDS data output buffers (LVDS DOBx16) accept 16-bit wide words from DMX1:16 and converts them into 16 LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. The block also provides a bit order selection under control of external CMOS signal "bitordn". The MSB is assigned to "q15" at "bitordn"="0" (default)or to "q00" at "bitordn"="1".

LVDS COB x2

The dual LVDS clock output buffer (LVDS COBx2) utilizes the same proprietary output buffers as in DOBx16. It receives two clock signals and converts them into LVDS output signals "clo" and "clm".

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Terminal Functions

The description of the package pins is presented in the table below.

Supply and Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply. (+3.3*V*)	5, 8, 11, 14, 25, 26, 29, 32, 35, 38, 41, 44, 52, 55, 59, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100
vee	Negative power supply. (GND or 0*V*)	1, 15, 23, 30, 36, 50, 51, 58, 75
nc	Unconnected pin.	74

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
dp	39	Input	CML differential data inputs with internal SE 50*Ohm* termination to “vtt”.
dn	40		
cep	33	Input	CML differential clock inputs with internal SE 50*Ohm* termination to “vcc”.
cen	34		
Controls			
bitordn	16	LS In., CMOS	Output bit order selection (default: high, “q15” is MSB; active: low, “q00” is MSB).
loln	19	LS Out, CMOS	CDR FWD lock indicator (high: locked; low: no lock).
ftr1	20	I/O	External CDR FWD filter connections.
ftr2	21		
oncml	24	LS In., CMOS	Low-speed input clock termination selection: (default: low, LVDS; active: high, CML).
vtt	31	DC In.	Adjustable termination voltage for DIP (default: 2.5*V*).
swf_20u	69	LS In., CMOS	Charge pump current selection (fwd current, off by default).
swf_m13	37	LS In., CMOS	Charge pump current selection (fwd current, off by default).
swf_m32	22	LS In., CMOS	Charge pump current selection (fwd current, off by default).
swa_m35	2	LS In., CMOS	Charge pump current selection (apd current, off by default).
offcdr	47	LS In., CMOS	Selects CDR or Digital mode of operation (default: low, CDR; active: high, Digital).
off0p	48	DC In.,	DATA IB thresholding.
off0n	49		
losn	53	LS Out, CMOS	Input data signal quality indicator (high: good; low: not good).
oncr16	54	LS In., CMOS	Activation of /4 block (default: low, cr = C/64, active: high, cr = C/16).
phs1	57	LS In., CMOS	Low-speed output clock “clo” phase selection (default: both low).
phs2	56		

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TERMINAL			DESCRIPTION
Pin Name	No.	Type	
Low-Speed I/Os			
crp	27	Input	LVDS or CML reference clock inputs for CDR FWD. Can be either C/16 or C/64.
crn	28		
q15n	10	Output	LVDS data outputs.
q15p	9		
q14n	7		
q14p	6		
q13n	4		
q13p	3		
q12n	99		
q12p	98		
q11n	96		
q11p	95		
q10n	93		
q10p	92		
q09n	90		
q09p	89		
q08n	87		
q08p	86		
q07n	84		
q07p	83		
q06n	81		
q06p	80		
q05n	78		
q05p	77		
q04n	73		
q04p	72		
q03n	70		
q03p	69		
q02n	67		
q02p	66		
q01n	64		
q01p	63		
q00n	61		
q00p	60		
clop	12	Output	LVDS clock outputs. Can transmit four different clock phases as defined by “phs1” and “phs2”.
clon	13		
clmp	17	Output	LVDS clock outputs.
clmn	18		
sldp	45	Output	Peak detector outputs.
sldn	46		

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ELECTRICAL CHARCTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
		General Parameters			
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
Power consumption		890		*mW*	
Junction temperature	-25	50	125	*°C*	
		HS Input Data (d)			
Data Rate	13.5		14.5	*Gbps*	
Swing (Diff or SE)	0.02		1.2	*V*	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
		HS Input Clock (ce)			
Frequency	0.0		15	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
		LS Input Reference Clock (cr)			
Frequency	219		875	*MHz*	C/64 or C/16
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
		LS Output Data (q00-q15)			
Data Rate	700		780	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		LS Output Clocks (clm, clo)			
Frequency	840		905	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
		Output of Peak Detector (sld)			
Swing (Diff)	0		0.6	*V*	Peak-to-peak over full input range
CM Voltage Level		Vcc-2.5		*V*	
		CMOS Control Inputs/Outputs			
Logic "1" level	V_{CC}-0.4			*V*	
Logic "0" level			V_{EE}+0.4	*V*	
		Timing Parameters			
"clm" and "clo" to "q0-q15" delay variation		±2.5%			Over the full temperature range

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package's mechanical information is available on the company's website.