ADSANTEC
Ultra High-Speed Mixed Signal ASICs
Advanced Science And Novel Technology Company, Inc.
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ASNT2016-PQA (ASNT2042)
1:16 CDR-DMUX

- 1:16 demultiplexer (DMUX) with integrated full rate CDR (clock and data recovery).
- Supports multiple data rates in the 11.3-12.5*Gbps* range in the CDR mode.
- Can operate in broadband digital mode up to 12.5*Gbps* with application of full rate clock.
- Supports both RZ and NRZ input data formats.
- LVDS output data buffers that feature a low-power proprietary architecture.
- Stable clock-divided-by-16 LVDS output with 90°-step phase selection.
- Supports clock-divided-by-16/64 input reference clock.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 730*mW* at 12.5*Gbps*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

DESCRIPTION

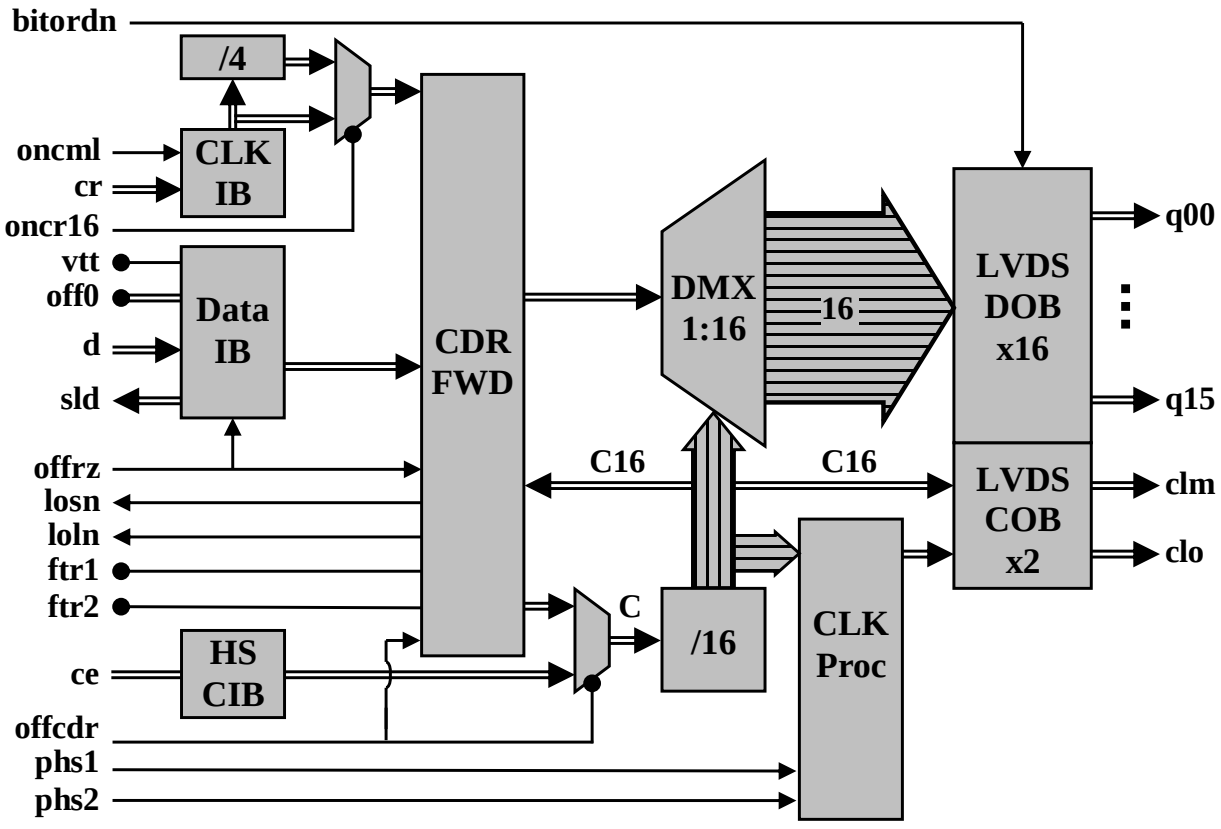

Fig. 1. Functional Block Diagram.

ASNT2016 is a 12.5*Gbps* 1:16 deserializer (DMUX) with full rate integrated clock and data recovery (CDR FWD). The DMUX can cover input data rates (f_{bit}) in the CDR mode from 11.3*Gbps* to 12.5*Gbps* by utilizing its on-chip full-rate VCO or function in the broadband digital mode. An external full clock "ce" must be applied to the high speed CML clock input buffer (HS CIB) for digital operation. Selection of the operational mode is made through pin "offcdr".

The main function of ASNT2016 is to demultiplex a serial input data channel "d" running at a bit rate of f_{bit} into 16 parallel data channels "q00-q15" running at a bit rate of $f_{bit}/16$. The high sensitivity CDR FWD block ensures accurate clock and data recovery for input data signal amplitudes greater than 20*mV* peak to peak (p-p) differential or single-ended. This is accomplished with the CDR FWD circuitry incorporating both a phase and frequency acquisition loop to recover a full rate clock "C" from the input data stream. This recovered clock samples the input data bits before they are demultiplexed and is also sent to the internal divider (/16).

The application of an external low speed system clock "cr" running at 1/16 or 1/64 the frequency of the VCO clock through the low speed clock input buffer (CLK IB) is required for CDR FWD to operate correctly. CLK IB by default provides a LVDS input interface, but can properly process input CML signaling through utilization of the "oncml" control signal. Pin "oncr16" selects between direct "cr" and "cr" post the divider-by-4 (/4) block.

The high-speed CML data input buffer (Data IB) and HS CIB provide on-chip 50*Ohm* termination and are designed to be driven by devices with 50*Ohm* source impedance. Data IB sets its termination voltage internally, but "vtt" can be used to externally adjust it if desired. Pins "off0" control the offset voltage between Data IB's "dp" and "dn" inputs allowing the user to change the slicing or threshold level at the serial data input. A peak detector is incorporated in Data IB to monitor the amplitude of the incoming data stream with its output made available through the differential pins "sld". Data IB can handle both RZ and NRZ input data formats.

The reconstructed serial input data is latched into the demultiplexer (DMX1:16) and is subsequently deserialized and delivered to the demultiplexer's output as 16-bit wide low-speed parallel words. Utilizing pin "bitordn", the deserializer can designate either "q00" or "q15" as the MSB thus simplifying the interface between ASNT2016 and a following ASIC.

Sixteen proprietary low-power LVDS output data buffers (LVDS DOBx16) are used to deliver the 16 data output signals "q00-q15" while a similar dual LVDS clock output buffer (LVDS COBx2) outputs the two low-speed clock signals "clm" and "clo". The buffers satisfy all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995 while only consuming 30*mW* each. The phase of "clo" can be modified by 90° increments by utilizing pins "phs1" and "phs2", which program the clock processing block (CLK Proc).

ASNT2016 includes alarm indicators loss of signal "losn" and loss of lock "loln". "offrz" must be activated when NRZ data is present for proper "losn" alarm generation. Off chip passive filter components are required by CDR FWD and are connected through pins "ftr1/2".

The deserializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

Data IB

The Data Input Buffer (Data IB) can process an input CML data signal "d" with bit rates up to 12.5*Gbps* in either the RZ or NRZ format. Data IB can also accept a single-ended signal to one of its input ports "dp" or "dn" with a threshold voltage applied to the opposite tuning pin "off0n" or "off0p". The tuning pins have input

impedances of 250*Ohm* and allow the user to change the slicing level before the data is sampled by the recovered clock. Data IB can handle input signal amplitudes between 20*mV* and 600*mV* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to "vtt"=2.5*V* (default) for each input line where "vtt" can be adjusted externally.

Also included in Data IB is an input signal peak detector that delivers its response through the output differential signal "sld". The detector can demodulate AM component(s) carried by the input data stream that are in the frequency range of up to a few hundred kHz. The peak detector's output impedance is 3.2*KOhm* single ended to Vcc.

CLK IB

The Clock Input Buffer (CLK IB) consists of a single proprietary universal input buffer (UIB). UIB is designed to accept differential signals with amplitudes higher than 60*mV* p-p, DC common mode voltage variation between the negative (vee) and positive (vcc) supply voltages, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes of more than 60*mV* p-p and threshold voltages between vee and vcc. By default, the input termination impedance is set to 100*Ohm* differential to support the LVDS standard. Correct impedance for the CML standard (50*Ohm* single ended to vcc) is set by applying logic "1" to "oncml".

/4

The divide-by-4 block (/4) is controlled by "oncr16" and is activated when "cr" is equal to the frequency of "C16". "oncr16" should be set to logic "0" (default) when "cr" is 1/4 the frequency of "C16". In both cases, a reference clock signal is delivered to CDR FWD with a frequency of 1/64 the rate of "C".

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can process an external CML clock signal "ce" with frequencies from 10.0*MHz* to 12.5*GHz*. It can also accept a single-ended signal to "cep/cen" with a threshold voltage applied to the unused "cen/cep" pin. HS CIB can handle input signal amplitudes between 200*mV* and 1.2*V* p-p differential or single-ended. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

CDR FWD

The Clock and Data Recovery Block (CDR FWD) contains both a phase and frequency acquisition loop that require a single off-chip filter featuring a 200*Ohm* resistor in series with a 1*nF* capacitor across the pins "ftr1" and "ftr2". The frequency loop works in concert with "cr" while the phase loop utilizes "d".

The main function of CDR FWD is to frequency lock the on-chip VCO to the input data signal (clock recovery) while phase aligning it to latch in the incoming data with minimal error (data recovery). The recovered clock is also utilized by /16 and DMX 1:16 to demultiplex the data.

CDR FWD raises the loss of signal "losn" flag when the input data's quality in RZ format is not sufficient enough for an acceptable bit error rate or the transition density of the data in either format is not enough or too much. By default, CDR FWD is set for RZ input data ("offrz"=0) where "offrz" must set to logic "1" when there is input NRZ signaling. A loss of lock "loln" is generated by CDR FWD when the frequency difference between a processed "cr" and "C" divided-by-64 is greater than ±1000*ppm*.

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/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock "C" delivered by CDR FWD is fed into the first divide-by-2 where its output is routed internally to the next divide-by-two circuit and outside of the block to DMX1:16. Other divided down clock signals are formed and routed to DMX1:16 in similar fashion. Full rate clock divided-by-16 "C16" is passed on to CLK Proc for additional phase adjustment as well as directly to a LVDS OB.

DMX1:16

The 1 to 16 Demultiplexer (DMX1:16) utilizes a tree type architecture that latches in the data stream from CDR FWD on both edges of a half rate clock signal that is supplied by /16. The high speed data signal is subsequently demultiplexed down and delivered to LVDS DOBx16 in parallel fashion as16-bit wide words running at a data rate up to 780*Mbps*.

CLK Proc

By utilizing the CMOS control pins "phs1" and "phs2", the phase of "clo" can be altered in accordance with the table below.

"phs1"	"phs2"	"clo" phase
V_{EE} (default)	V_{EE} (default)	270°
V_{EE}	V_{CC}	180°
V_{CC}	V_{EE}	90°
V_{CC}	V_{CC}	0°

LVDS DOBx16

The LVDS Data Output Buffer (LVDS DOBx16) accepts 16-bit wide words from DMX1:16 and converts them into LVDS output signals. Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at bit rates up to 2*Gb/s* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. When "bitordn"=0 (default), "q15"is the MSB and when "bitordn"=1, "q00" is designated the MSB.

LVDS COB x2

The dual LVDS Clock Output Buffer (LVDS COB x2) receives two clock signals and converts them into the LVDS output signals "clm" and "clo". Each proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

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Terminal Functions

The description of the package pins is presented in the table below.

TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
crp	27	Input	LVDS or CML reference clock inputs for CDR FWD. Can be either C/16 or C/64.
crn	28		
q00n	10	Output	LVDS data outputs.
q00p	9		
q01n	7		
q01p	6		
q02n	4		
q02p	3		
q03n	99		
q03p	98		
q04n	96		
q04p	95		
q05n	93		
q05p	92		
q06n	90		
q06p	89		
q07n	87		
q07p	86		
q08n	84		
q08p	83		
q09n	81		
q09p	80		
q10n	78		
q10p	77		
q11n	73		
q11p	72		
q12n	70		
q12p	69		
q13n	67		
q13p	66		
q14n	64		
q14p	63		
q15n	61		
q15p	60		
clop	12	Output	LVDS clock outputs. Can transmit four different clock phases

clon	13		as defined by "phs1" and "phs2".
clmp	17	Output	LVDS clock outputs.
clmn	18		
sldp	45	Output	Peak detector outputs.
sldn	46		
High-Speed I/Os			
dp	39	Input	CML differential data inputs with internal SE 50*Ohm* termination to "vtt".
dn	40		
cep	33	Input	CML differential clock inputs with internal SE 50*Ohm* termination to "vcc".
cen	34		
Controls			
bitordn	16	LS In., CMOS	Output bit order selection (default: high, q15 is MSB; active: low, q00 is MSB).
loln	19	LS Out, CMOS	CDR FWD lock indicator (high: locked; low: no lock).
ftr1	20	I/O	External CDR FWD filter connections.
ftr2	21		
oncml	24	LS In., CMOS	Low-speed input clock termination selection: (default: low, LVDS; active: high, CML).
vtt	31	DC In.	Termination voltage for Data IB (default: 2.5*V*). Can be adjusted externally to desired value.
offrz	37	LS In., CMOS	Input data format selection (default: low, RZ data; active: high, NRZ data).
offcdr	47	LS In., CMOS	Selects CDR or Digital mode of operation (default: low, CDR; active: high, Digital).
off0p	48	DC In.,	DATA IB thresholding.
off0n	49		
losn	53	LS Out, CMOS	Input data signal quality indicator (high: good; low: not good).
oncr16	54	LS In., CMOS	Activation of /4 block (default: low, cr = C/64, active: high, cr = C/16).
phs1	57	LS In., CMOS	Low-speed output clock "clo" phase selection (default: both low).
phs2	56		

Supply and Termination Voltages

Name	Description	Pin Number
vcc	Positive power supply. (+3.3*V*)	5, 8, 11, 14, 25, 26, 29, 32, 35, 38, 41, 44, 52, 55, 59, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100.
vee	Negative power supply. (GND or 0*V*)	1, 15, 23, 30, 36, 50, 51, 58, 75.
nc	Unconnected pin.	2, 22, 42, 43.

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ELECTRICAL CHARCTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
V_{CC}	+3.14	+3.3	+3.47	*V*	±5%
V_{EE}		0.0		*V*	
Power consumption		730		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Data (dp/dn)					
Data Rate	11.3		12.5	*Gbps*	
Swing (Diff or SE)	0.02		1.2	*V*	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
HS Input Clock (cep/cen)					
Frequency	0.0		12.5	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	V_{CC}-0.8		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
LS Input Reference Clock (crp/crn)					
Frequency	350		780	*MHz*	C/64 or C/16
Swing (Diff or SE)	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	V_{EE}		V_{CC}	*V*	
Duty Cycle	40%	50%	60%		
LS Output Data (q00p/q00n-q15p/q15n)					
Data Rate	700		780	*Mbps*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
LS Output Clocks (clmp/clmn, clop/clon)					
Frequency	700		780	*MHz*	
Interface		LVDS			Meets the IEEE Std. 1596.3-1996
Output of Peak Detector (sldp/sldn)					
Swing (Diff)	0		0.6	*V*	Peak-to-peak over full input range
CM Voltage Level		Vcc-2.5		*V*	
CMOS Control Inputs/Outputs					
Logic “1” level	V_{CC}-0.4			*V*	
Logic “0” level			V_{EE}+0.4	*V*	
Timing Parameters					
“clm” and “clo” to “q0-q15” delay variation		±2.5%			Over the full temperature range

PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package.

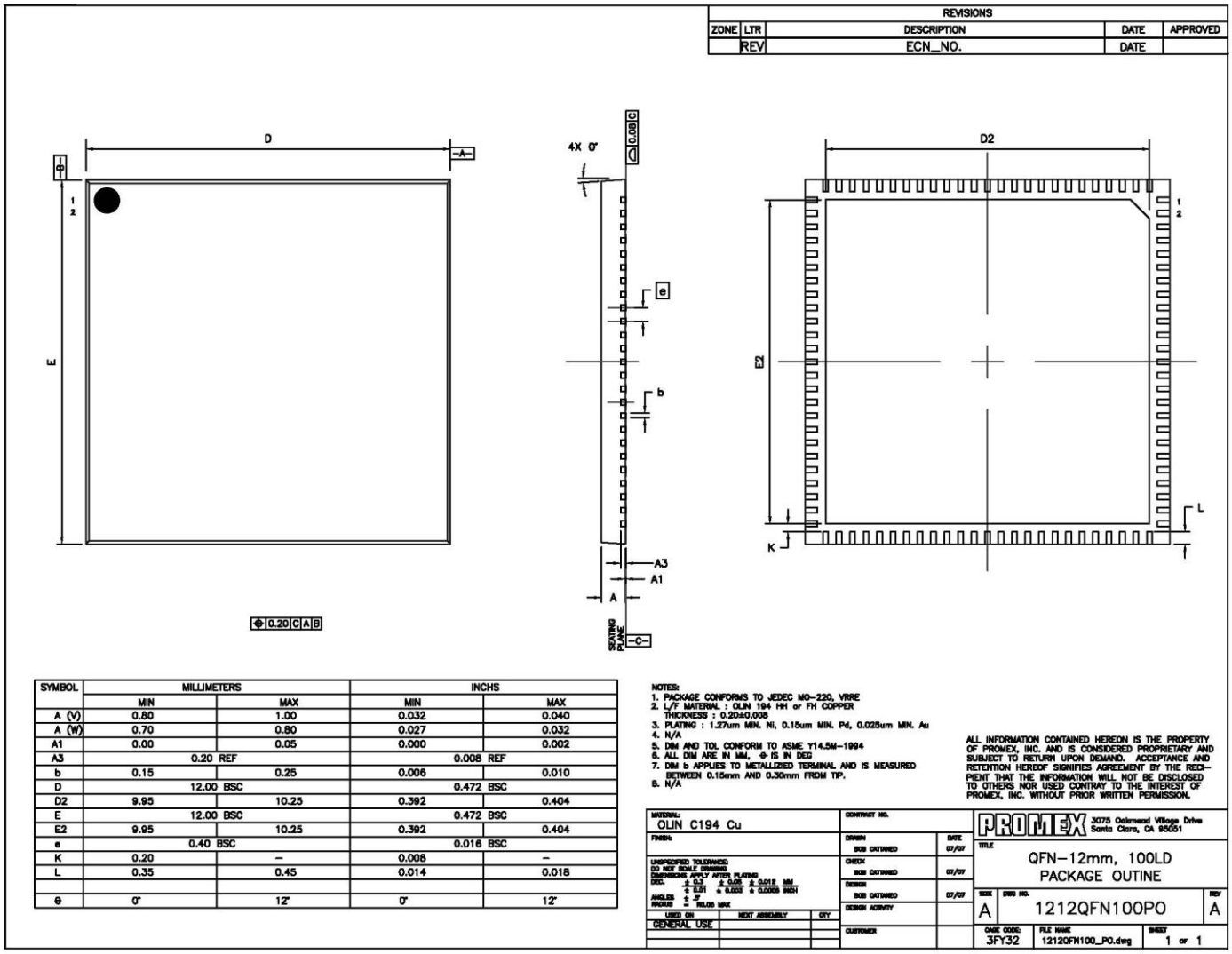

Fig. 2. Package Drawing

The chip die is housed in a custom 100-pin CQFP package shown in Fig. . Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the **vee** plain that is ground for the positive supply.

The part's identification label is ASNT2016-PQA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
2.2.2	05-2020	Updated Package Information
2.1.1	07-2019	Updated Formatting and Letterhead
1.0	03-2011	First release