ADSANTEC
Ultra High-Speed Mixed Signal ASICs
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# ASNT1017
# 16:1 MUX-CMU

- 16 to 1 multiplexer (MUX) with integrated CMU (clock multiplication unit).
- Supports data rates from 11.5*Gb/s* to 14.5*Gb/s* in CMU mode.
- LVDS compliant input data buffers.
- Selectable full-speed or divided-by-2 clock output.
- LVDS output clock-divided-by-16 with a selectable phase.
- Single +3.3*V* power supply.
- Industrial temperature range.
- Low power consumption of 500*mW*.
- Available in standard 100-pin QFN package (12*mm* x 12*mm*).

## *DESCRIPTION*

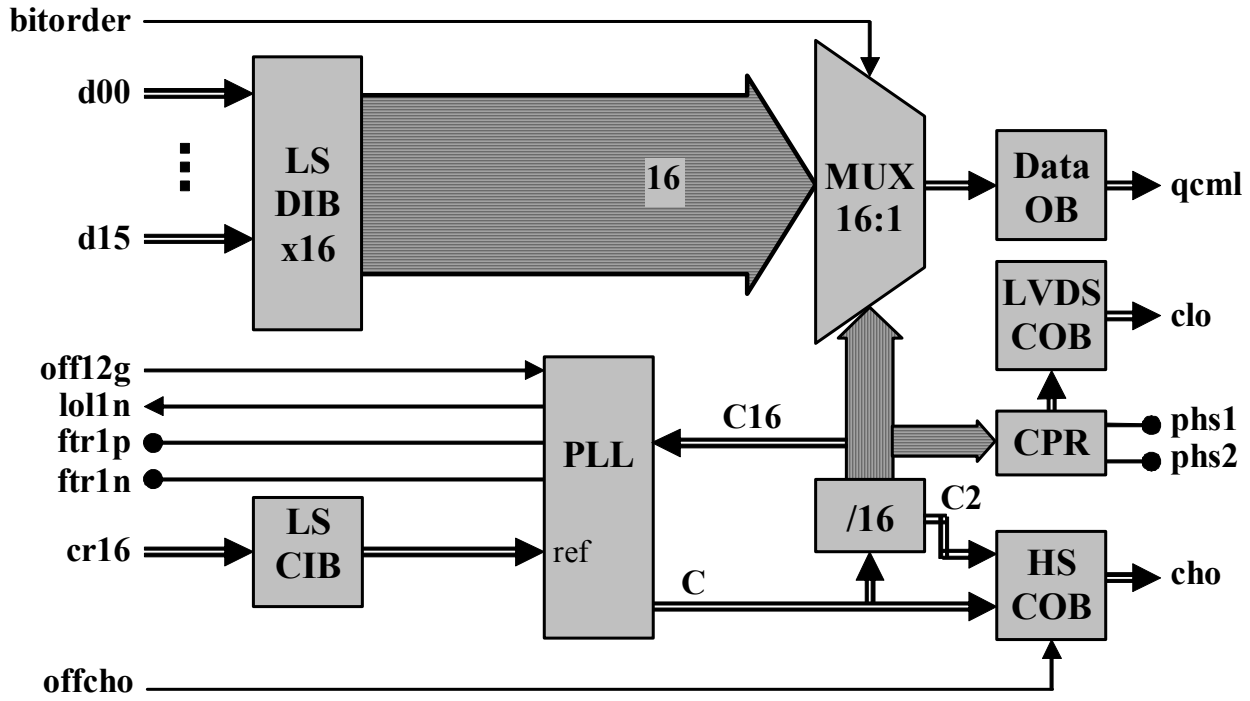


*Fig. 1. Functional Block Diagram.*

ASNT1017 is a low power and high-speed 16-to-1 multiplexer (MUX) with an internal clock multiplier unit (CMU). The main function of the chip is to multiplex 16 parallel data channels running at a bit rate of $f_{bit}/16$ into a high-speed serial bit stream running at $f_{bit}$. It provides a high-speed output data channel for point-to-point data transmission over a 50*Ohm* controlled impedance media. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

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During normal operation, the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words "d00"-"d15" through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. By utilizing pin "bitorder", the serializer can designate either "d00" or "d15" as the MSB thus simplifying the interface between the multiplexer and the digital data source.

MUX16:1 serializes the data words with multiple divided down clock signals that are generated from the full rate clock "C" by the internal divider (/16). The divider also produces half rate clock "C2" for the high speed clock output buffer (HS COB), and engenders a full rate clock divided-by-16 signal "C16" for use by the PLL (PLL). "C" is synthesized by PLL, which locks "C16" to the external system level clock "cr16" that is provided by the low speed clock input buffer (LS CIB). "cr16" must be 1/16 the frequency of the active full rate VCO in PLL. PLL contains 2 full rate VCOs to cover the frequency range from 11.5*Gbps* to 14.5*Gbps*, which are selected utilizing the "off12g" control pin. It also generates a loss-of-lock alarm signal "lol1n".

The serialized words are transmitted as 2-level signals "qcml" by a differential CML output buffer (Data OB). A full-rate or half-rate clock "cho" is transmitted by a similar CML buffer (HS COB) in parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. HS COB may be disabled or its operational mode changed by means of the 3-state (vee, vcc, not connected (n/c)) CMOS "offcho" signal. Both output stages are back terminated with on-chip 50*Ohm* resistors.

The chip also provides a differential low speed output clock "clo" though a LVDS clock output buffer (LVDS COB). The 0º, 90º, 180º, or 270º phase of the clock signal can be selected using control pins "phs1" and "phs2" as shown in Table 1.

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

## LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that fully comply with the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative (vee) and positive (vcc) supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV* p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100*Ohm* differential.

## LS CIB

The Low-Speed Clock Input Buffer (LS CIB) is a UIB that can run at a frequency up to 800*MHz*. This block is used to deliver the low speed system clock "cr16" as a reference signal to PLL.

## PLL

The Phase Locked Loop (PLL) contains a phase frequency detector, charge pump, an on-chip integrator with an additional off-chip filter connected between the pins "ftr1p" and "ftr1n" (Fig. 2), and two selectable LC-tank VCOs centered at 14*GHz* and 12*GHz*. The main function of PLL is to synthesize full rate clock "C" by aligning the phase and frequency of "C16" of the activated VCO to the externally applied system clock "cr16". A logic "0" output CMOS loss-of-lock "lol1n" alarm signal is generated by PLL if its two input clock signals are not matching in phase and/or frequency.


*Fig. 2. External Filter Schematic.*

Selection of the different VCOs of PLL is achieved by utilizing the CMOS control pin "off12g". A logic "1" chooses the 12*GHz* VCO while a logic "0" selects the 14*GHz* VCO (default state). The unused VCO is turned completely off in order to save power.

## /16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. High-speed clock "C" is fed into the first divide-by-2 circuit that generates "C2". "C2" is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1 and HS COB. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. "C16" is passed on to PLL and LVDS COB to become the output low speed clock signal "clo".

## MUX16:1

The 16 to 1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the "C16" clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a serial data stream running at a data rate up to 15*Gbps*. The latency of this circuit block is equal to roughly one period of the low-speed input clock. When "bitorder"=0 (default), "d00"is the MSB and when "bitorder"=1, "d15" is designated the MSB.

## Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into the CML output signal "qcml" with a single ended swing of 600*mV*. The buffer requires 50*Ohm* external termination resistors connected between "vcc" and each output to match its internal 50*Ohm* resistors and can operate at a data rate up to 15G*bps*.

## HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB and can operate at a frequency up to 15*GHz* while producing a single-ended CML output swing of 600*mV*. The buffer can be enabled or disabled by the external 3-state (vcc, vee, not connected (n/c)) control signal "offcho". The n/c default state corresponds to a "C2" output signal. The logic "0" state provides a full-rate clock output signal while the logic "1" state disables the buffer completely to save power.

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## CLK Proc

By utilizing the CMOS control pins "phs1" and "phs2", the phase of the output low-speed clock ("clo") can be selected in accordance with Table 1 below.

*Table 1. Output Clock Phase Selection.*

| "phs1" | "phs2" | C16 phase |
|---|---|---|
| $V_{EE}$ (default) | $V_{EE}$ (default) | 270° |
| $V_{EE}$ | $V_{CC}$ | 180° |
| $V_{CC}$ | $V_{EE}$ | 90° |
| $V_{CC}$ | $V_{CC}$ | 0° |

## LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives a signal from the clock processor and converts it into an LVDS output signal "clo". The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2*GHz* with a low power consumption level of 30*mW*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

## Output Timing

Phase relation between the output data "qcml" and full rate output clock "cho" is specified in Table 2 and illustrated by Fig. 3.

*Table 2. Output Data-to-Clock Phase Difference*

| Junction temperature, *°C* | **τ**, *ps* | |
|---|---|---|
| | Min. | Max. |
| -25 | 77 | 80 |
| 50 | 82 | 86 |
| 125 | 87 | 91 |

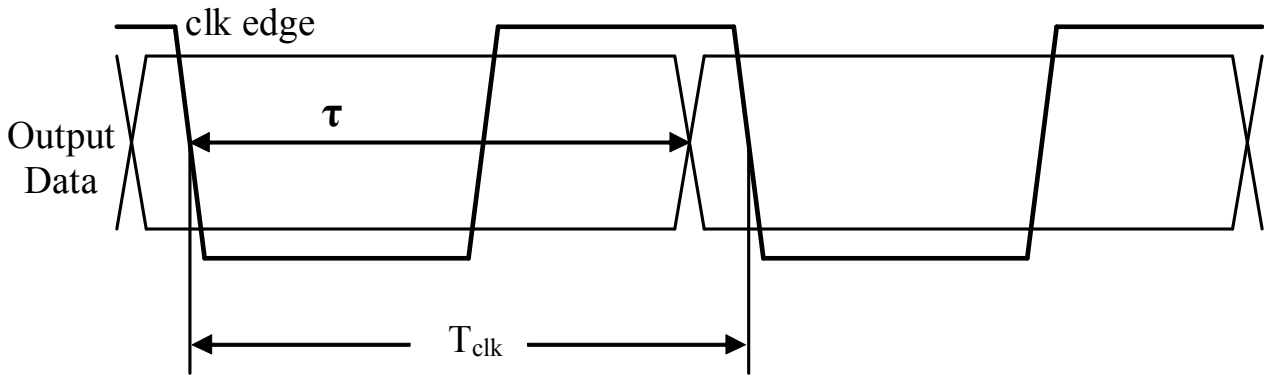


*Fig. 3. Output Timing Diagram.*

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# *TERMINAL FUNCTIONS*

The description of the package pins is presented in the table below.

| ***Supply and Termination Voltages*** | | |
|---|---|---|
| **Name** | **Description** | **Pin Number** |
| vcc | Positive power supply. (+3.3*V*) | 5, 8, 11, 25, 26, 29, 32, 35, 38, 41, 44, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100. |
| vee | Negative power supply. (GND or 0*V*) | 1, 15, 23, 24, 30, 36, 50, 51, 75, |
| vecl | Input termination voltage. ("vcc" for CML, +2*V* for ECL) | 2 and 74. |
| nc | Unconnected pin. | 17, 27, 28, 31, 42, 43, 47-49, 52-54, 58. |

| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| Name | No. | Type | |
| ***High-Speed I/Os*** | | | |
| chop | 34 | Output | CML differential clock outputs. Require external SE 50*Ohm* termination to "vcc". Can be disabled by "offcho". |
| chon | 33 | | |
| qcmlp | 40 | Output | CML differential data outputs. Require external SE 50*Ohm* termination to "vcc". |
| qcmln | 39 | | |
| ***Controls*** | | | |
| lol1n | 19 | LS Out, CMOS | PLL1 lock indicator (high: locked; low: no lock). |
| ftr1p | 20 | I/O | PLL1 external filter connection (1*nF* capacitor differential). |
| ftr1n | 21 | | |
| offecl | 14 | LS In., CMOS | LS input termination selector (active: low, CML or ECL depending on the "vecl" connection; default: high, LVDS). |
| offc64 | 16 | LS In., CMOS | Division ratio clock selection (active: low, division by 64; default: high, division by 16). |
| offcho | 18 | LS In., CMOS | HS COB control (active: high, buffer is disabled; default: low, full-rate output clock). |
| off12g | 22 | LS In., 3-state | VCO frequency selection (active: high, 11.0*GHz*; default: low, 11.8*GHz*). |
| capsel1 | 37 | LS In., CMOS | Internal filter select (default: n/c, 22.5*pF*; high: 48*pF*, low: 10*pF*). |
| phs1 | 57 | LS In., CMOS | Low-speed output clock phase selection (default: both low). |
| phs2 | 56 | | |
| bitorder | 59 | LS In., CMOS | Input bit order selection (active: high, d15 is serialized first; default: low, d00 is serialized first). |

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| TERMINAL | | | DESCRIPTION |
|---|---|---|---|
| Name | No. | Type | |
| ***Low-Speed I/Os*** | | | |
| cr16p | 12 | Input | LVDS clock inputs. |
| cr16n | 13 | | |
| clop | 46 | Output | LVDS clock outputs. |
| clon | 45 | | |
| d00p | 60 | Input | LVDS data inputs. |
| d00n | 61 | | |
| d01p | 63 | | |
| d01n | 64 | | |
| d02p | 66 | | |
| d02n | 67 | | |
| d03p | 69 | | |
| d03n | 70 | | |
| d04p | 72 | | |
| d04n | 73 | | |
| d05p | 77 | | |
| d05n | 78 | | |
| d06p | 80 | | |
| d06n | 81 | | |
| d07p | 83 | | |
| d07n | 84 | | |
| d08p | 86 | | |
| d08n | 87 | | |
| d09p | 89 | | |
| d09n | 90 | | |
| d10p | 92 | | |
| d10n | 93 | | |
| d11p | 95 | | |
| d11n | 96 | | |
| d12p | 98 | | |
| d12n | 99 | | |
| d13p | 3 | | |
| d13n | 4 | | |
| d14p | 6 | | |
| d14n | 7 | | |
| d15p | 9 | | |
| d15n | 10 | | |

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# ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT | COMMENTS |
|---|---|---|---|---|---|
| | | ***General Parameters*** | | | |
| $V_{CC}$ | +3.14 | +3.3 | +3.47 | *V* | ±5% |
| $V_{EE}$ | | 0.0 | | *V* | |
| Power consumption | | 500 | | *mW* | |
| Junction temperature | -25 | 50 | 125 | *°C* | |
| | | ***LS Input Data (d00-d15)*** | | | |
| Data Rate | 720 | | 910 | *Mbps* | |
| Differential Swing | 0.06 | | 0.8 | *V* | Peak-to-peak |
| CM Voltage Level | $V_{EE}$ | | $V_{CC}$ | *V* | |
| | | ***LS Input Reference Clock (cr16)*** | | | |
| Frequency | 720 | | 910 | *MHz* | |
| Differential Swing | 0.06 | | 0.8 | *V* | Peak-to-peak |
| CM Voltage Level | $V_{EE}$ | | $V_{CC}$ | *V* | |
| | | ***HS Output Data (qcml)*** | | | |
| Data Rate | 11.5 | | 14.5 | *Gbps* | |
| Logic "1" level | | $V_{CC}$ | | *V* | |
| Logic "0" level | | $V_{CC}$-0.6 | | *V* | |
| Jitter | | 12 | | *ps* | Peak-to-peak @12.5*Gb/s* |
| | | ***HS Output Clock (cho)*** | | | |
| Frequency | 5.75 | | 14.5 | *GHz* | |
| Logic "1" level | | $V_{CC}$ | | *V* | |
| Logic "0" level | | $V_{CC}$-0.6 | | *V* | |
| Jitter | | 5 | | *ps* | Peak-to-peak @12.5*GHz* |
| Duty Cycle | | 50% | | | |
| | | ***LS Output Clock (clo)*** | | | |
| Frequency | 720 | | 910 | *MHz* | |
| Interface | | LVDS | | | Meets the IEEE Std. |
| | | ***CMOS Control Inputs/Outputs*** | | | |
| Logic "1" level | $V_{CC}$-0.4 | | | *V* | |
| Logic "0" level | | | $V_{EE}$+0.4 | *V* | |

# PACKAGE INFORMATION

The chip is packaged in a standard 100-pin QFN package. The package's mechanical information is available on the company's website.